

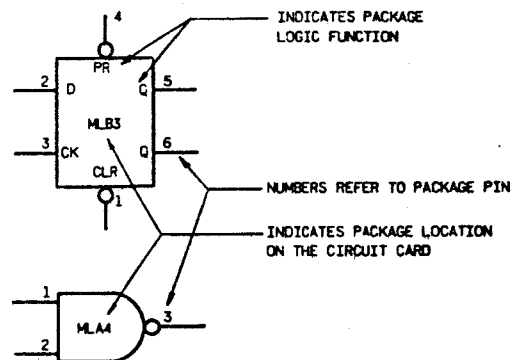
SHEET INDEX

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		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
SHEET INDEX, SUPPORTING INFORMATION	1	1	2	3	4																						1
BLOCK DIAGRAM	2	1	1	1	2																						2
FS-1 BUS INTERFACE AND REGISTER FILE	3	1	1	1	1																						3
FS-2 'A' MULTIPLEXER - LO BYTE	4	1	2	3	3																						4
FS-3 'A' MULTIPLEXER - HI BYTE AND 800X MULTIPLEXER	5	1	1	1	1																						5
FS-4 ARITHMETIC AND LOGIC UNIT, ACCUMULATOR, AND CARRY IN MULTIPLEXER	6	1	1	1	1																						6
FS-5 STATUS MULTIPLEXER & REGISTER & RUN LIGHT TIME	7	1	1	1	1																						7
FS-6 POWER AND FILTER CIRCUITS	8	1	1	1	1																						8
TC-1	9	1	1	1	1																						9
TC-2	10	1	1	1	1																						10
TC-3	11	1	1	1	1																						11
TC-4	12	1	1	1	1																						12

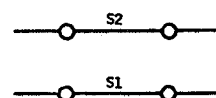
NOTES:

1. THE VOLTAGE, +5V, IS APPLIED TO PIN 8 OF THE 8 PIN PACKAGE, PIN 14 OF 14 PIN PACKAGES, PIN 16 OF 16 PIN PACKAGES, AND PIN 24 OF 24 PIN PACKAGES. GROUND IS APPLIED TO PIN 4 OF THE 8 PIN PACKAGE, PIN 7 OF 14 PIN PACKAGES, PIN 8 OF 16 PIN PACKAGES, AND PIN 12 OF 24 PIN PACKAGES.

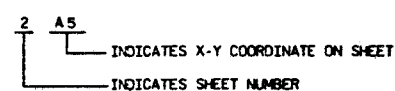
2. LOGIC NOTATION



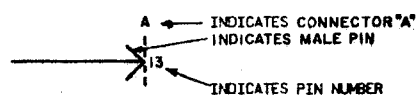
3. OPTION STRAP



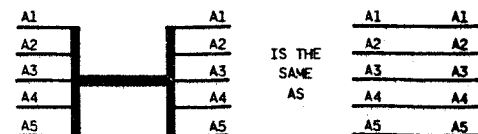
4. SHEET LOCATION CODE



5. CONNECTOR CODE



6. THE FOLLOWING INTERCONNECTION METHOD IS USED TO CONSERVE SPACE ON LEADS PERFORMING SIMILAR FUNCTIONS.



7. CONNECTOR PIN ASSIGNMENT

CONNECTOR	PIN	DESCRIPTION	SHEET LOCATION
A	25	D/A (8)	3A1
A	27	D/A (1)	3A1
A	29	D/A (2)	3A1
A	31	D/A (3)	3A1
A	33	D/A (4)	3B1
A	35	D/A (5)	3C1
A	37	D/A (6)	3C1
A	39	D/A (7)	3C1
A	41	D/A (8)	3C1
A	43	D/A (9)	3C1
A	45	D/A (10)	3C1
A	47	D/A (11)	3D1
A	49	D/A (12)	3E1
A	51	D/A (13)	3E1
A	53	D/A (14)	3E1
A	55	D/A (15)	3E1
A	68	+5V	8B1
A	69	+5V	8B1
A	70	0V	8D1
A	71	0V	8D1

8. ALL CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT DESCRIPTION	440000

USE OF SHEET INDEX

ANY CHANGES TO THIS INDEX ARE MADE IN THE INDEX SHEET. THE INDEX SHEET IS THE ONLY SOURCE FOR THE LATEST ISSUE OF THE INDEX SHEET.

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	3-18-75	23856-R
2	8-18-75	14543
3	2-17-76	16055
4	10-25-78	22076RC

9. ALL RESISTANCE VALUES IN OHMS UNLESS OTHERWISE SPECIFIED

10. $V_L = 0V$ TO $+0.4V$
 $V_H = +2.4V$ TO $5.5V$

11. LOGIC SYMBOLS:

- V = LOGIC OR
A = LOGIC AND
* = LOGIC EXCLUSIVE OR

12. TIMING CHARTS:

- ///// = INDETERMINATE
NOT LOGIC 1 OR LOGIC 0

SCHEMATIC DIAGRAM
FOR
INSTRUCTION
EXECUTION
LOGIC/A
CARD ASSEMBLY

APPROVALS

PROJ. SUPV.	PROJ. MFG. REL. COMPL.
<i>[Signature]</i>	<i>[Signature]</i>
ENGR. S.A.	DSGMR. J.D.
DRN. FILE	DATE 2/15/76
R&D FILE	6-167.172AA
S-NUMBER	

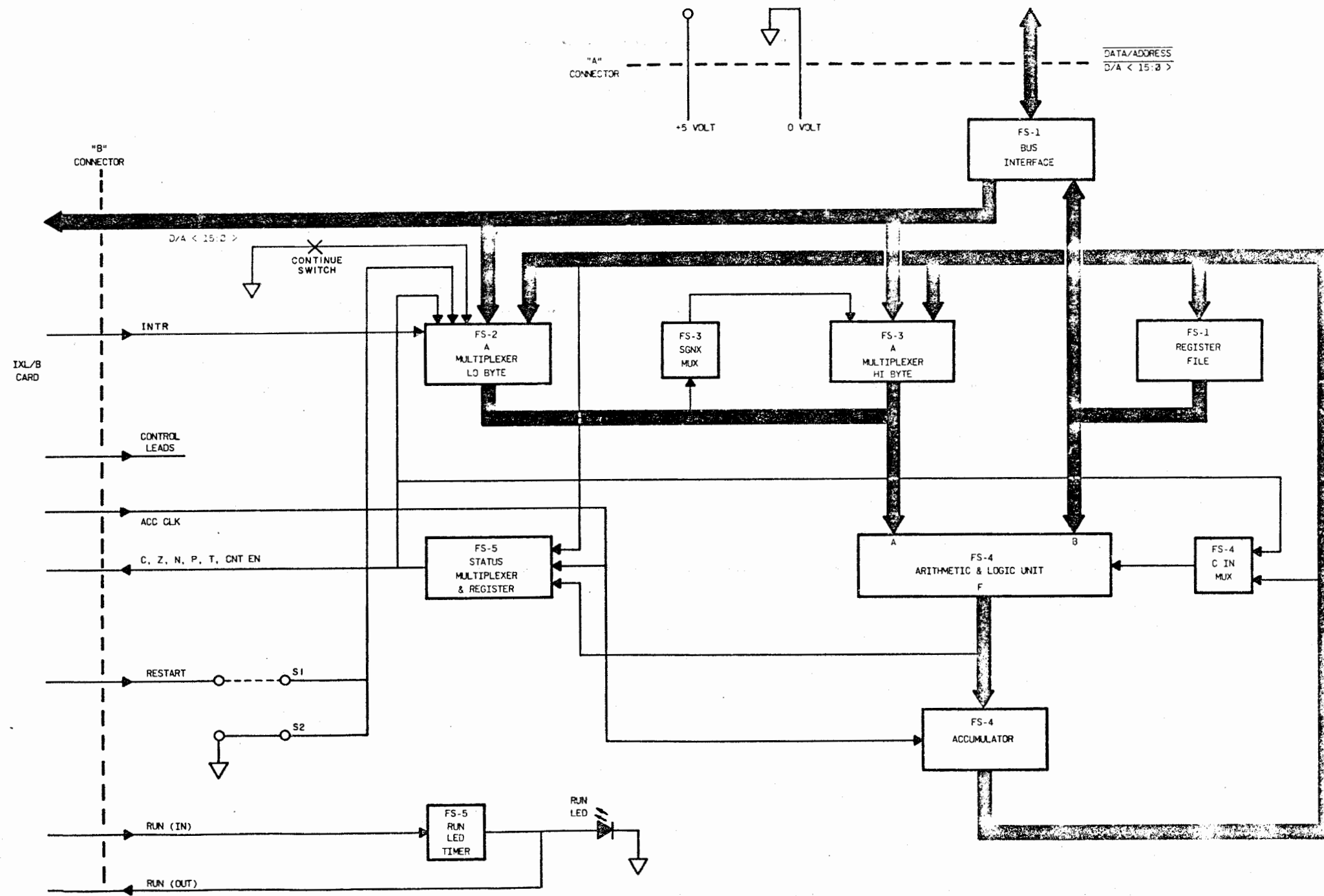
TELETYPE



4400SD-1

BLOCK DIAGRAM

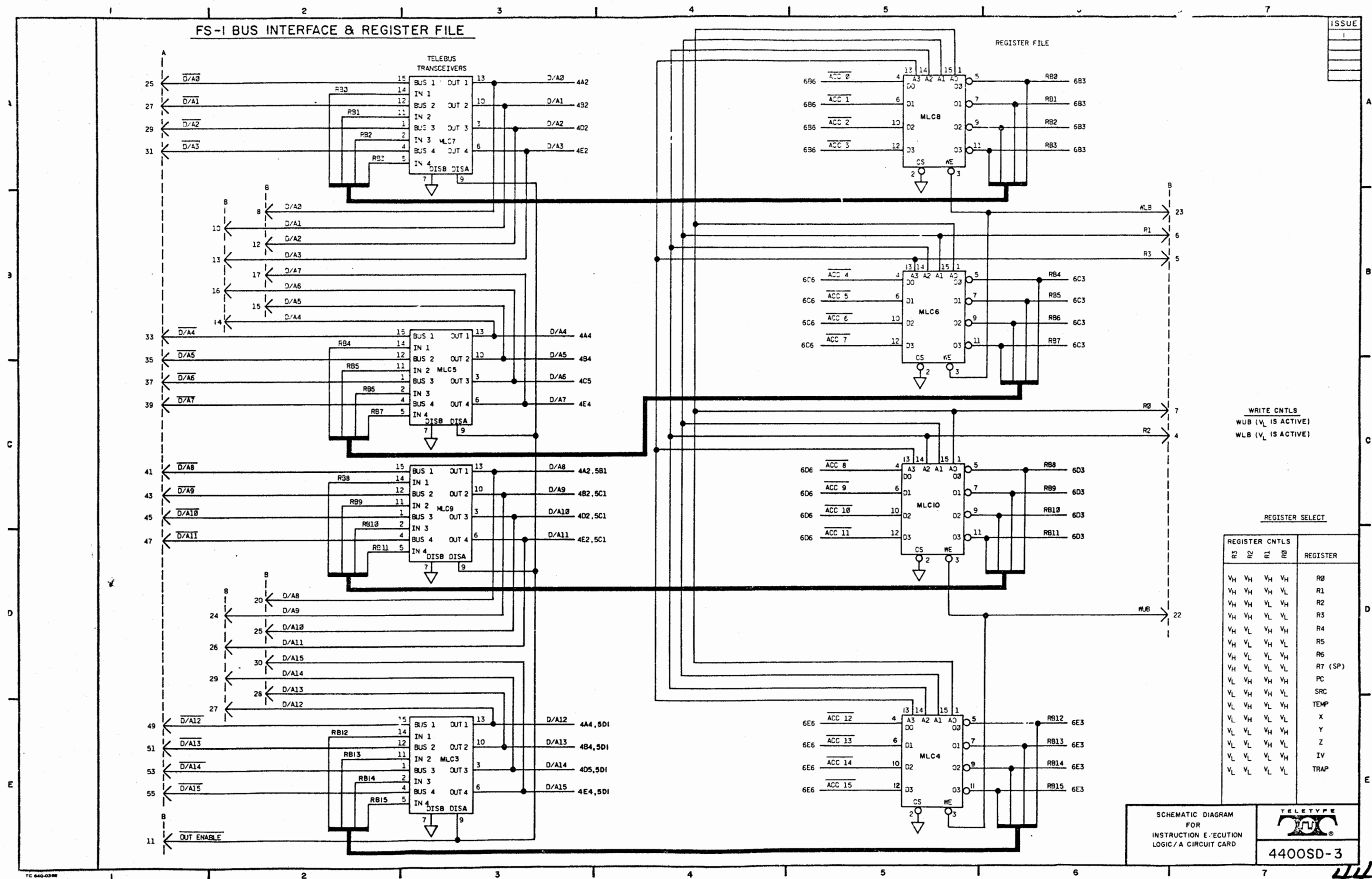
ISSUE
1
2



SCHEMATIC DIAGRAM
FOR
INSTRUCTION EXECUTION
LOGIC /A CIRCUIT CARD

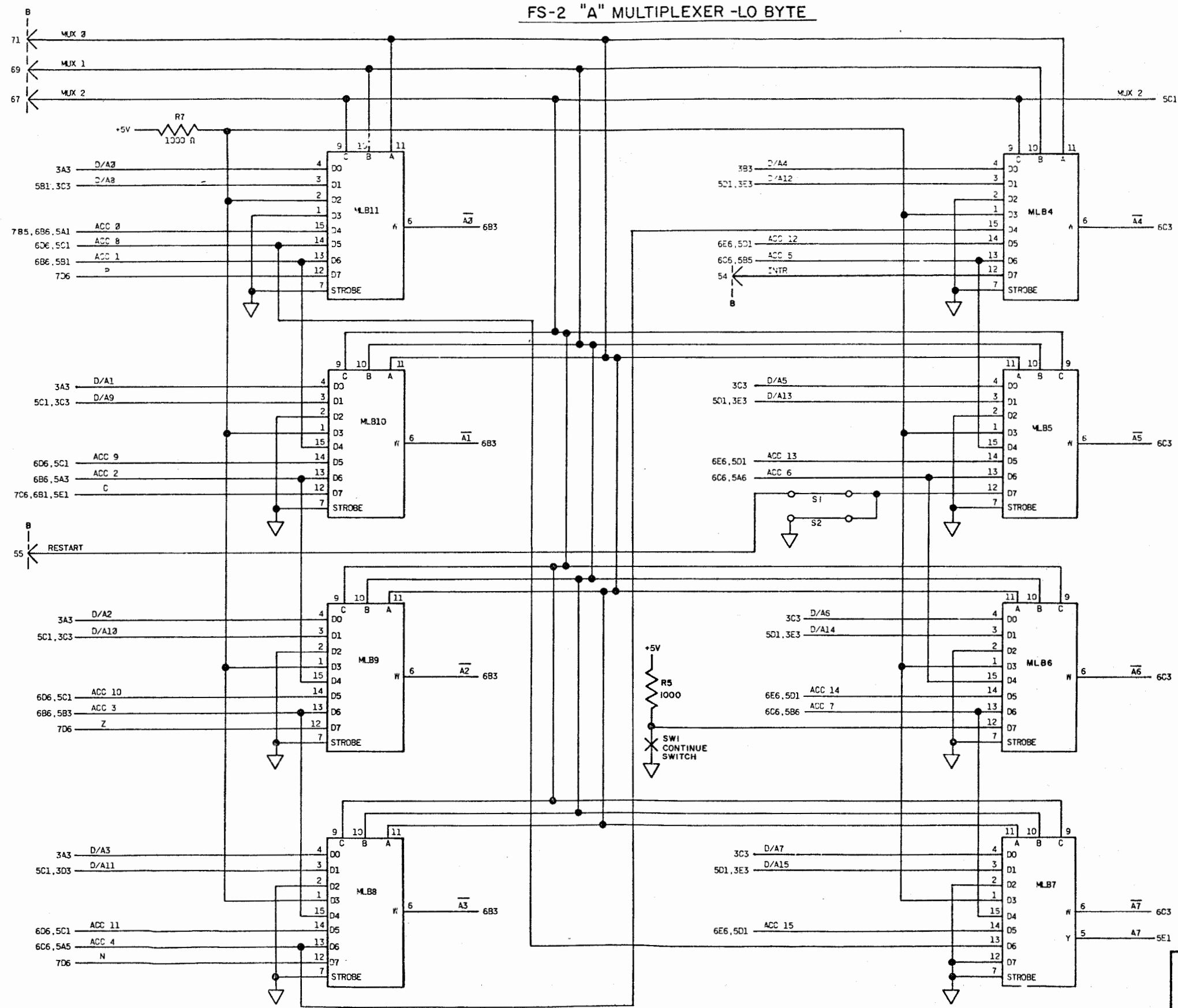


4400SD-2



FS-2 "A" MULTIPLEXER -LO BYTE

ISSUE
1
2
3



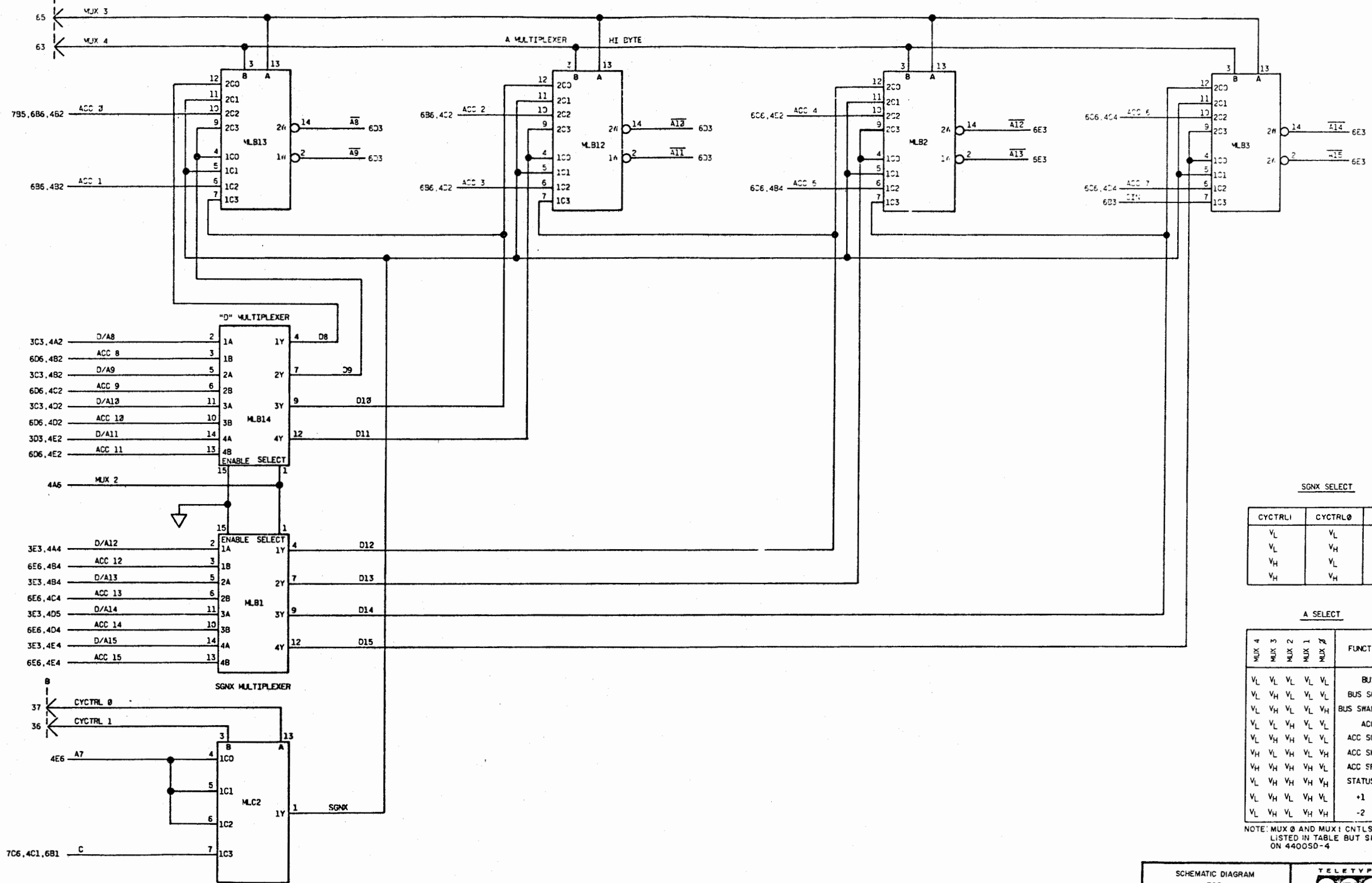
A SELECT			FUNCTION
MUX 2	MUX 1	MUX 0	
V _L	V _L	V _L	BUS
V _L	V _L	V _H	BUS SWAB SGNX
V _L	V _H	V _L	+1
V _L	V _H	V _H	-2
V _H	V _L	V _L	ACC
V _H	V _L	V _H	ACC SWAB
V _H	V _H	V _L	ACC - SR
V _H	V _H	V _H	STATUS

SCHEMATIC DIAGRAM
FOR
INSTRUCTION EXECUTION
LOGIC/A CIRCUIT CARD



4400SD-4

FS-3 "A" MULTIPLEXER-HI BYTE & SGNX MULTIPLEXER



SGNX SELECT

CYCTRL1	CYCTRL0	SGNX
V _L	V _L	A7
V _L	V _H	A7
V _H	V _L	A7
V _H	V _H	CSTAT

A SELECT

MUX 4	MUX 3	MUX 2	MUX 1	MUX 0	FUNCTION
V _L	V _L	V _L	V _L	V _L	BUS
V _L	V _H	V _L	V _L	V _L	BUS SGNX
V _L	V _H	V _L	V _H	V _L	BUS SWAB SGNX
V _L	V _L	V _H	V _L	V _L	ACC
V _L	V _H	V _H	V _L	V _L	ACC SGNX
V _H	V _L	V _H	V _L	V _H	ACC SWAB
V _H	V _H	V _H	V _H	V _L	ACC SR
V _L	V _H	V _H	V _H	V _H	STATUS
V _L	V _H	V _L	V _H	V _L	+1
V _L	V _H	V _L	V _H	V _H	-2

NOTE: MUX 0 AND MUX 1 CNTLS ARE LISTED IN TABLE BUT SHOWN ON 4400SD-4

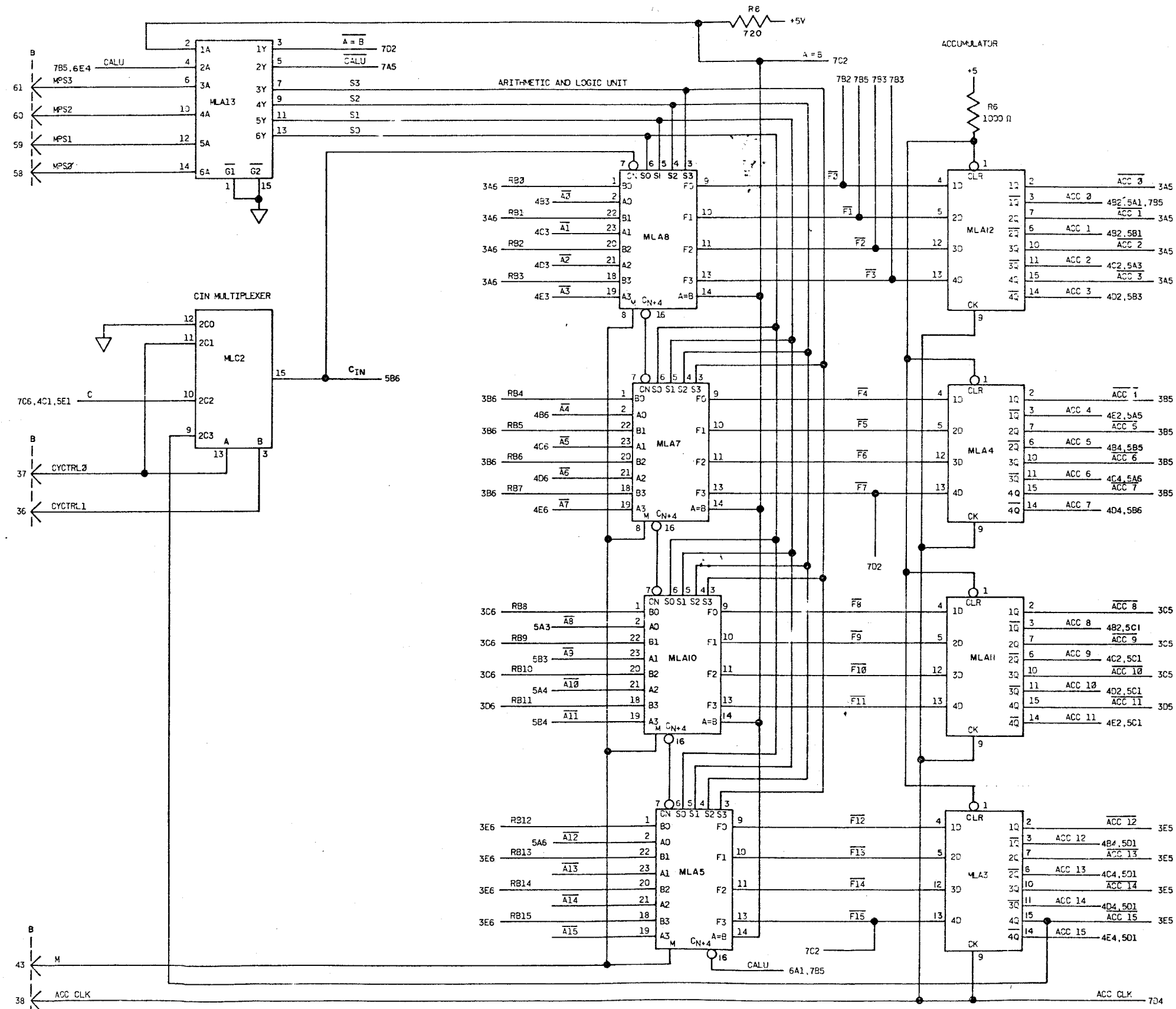
SCHEMATIC DIAGRAM
FOR
INSTRUCTION EXECUTION
LOGIC / A CIRCUIT CARD



4400SD-5

FS-4 ARITHMETIC AND LOGIC UNIT, ACCUMULATOR, & CARRY IN MULTIPLEXER

ISSUE
1



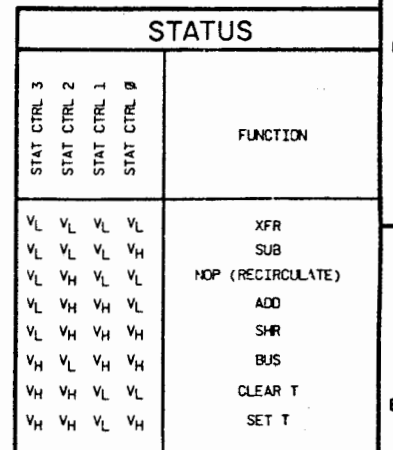
CARRY IN SELECT		
CYCTRL1	CYCTRL0	CIN
V _L	V _L	0
V _L	V _H	1
V _H	V _L	CSTAT
V _H	V _H	ACC 15

ALU OPERATIONS	
S3 S2 S1 S0	M = V _L - ARITHMETIC OPER. M = V _H - LOGIC OPER.
V _H V _H V _H V _H	A + CIN
V _H V _H V _H V _L	A + A + B + CIN
V _H V _H V _L V _H	A + A + B + CIN
V _H V _H V _L V _L	A + A + CIN
V _H V _L V _H V _H	(A + B) + CIN
V _H V _L V _H V _L	(A + B) + (A + B) + CIN
V _H V _L V _L V _H	A - B - CIN
V _H V _L V _L V _L	A + (A + B) + CIN
V _L V _H V _H V _H	(A + B) + CIN
V _L V _H V _H V _L	A + B + CIN
V _L V _H V _L V _H	(A + B) + (A + B) + CIN
V _L V _H V _L V _L	A + (A + B) + CIN
V _L V _L V _H V _H	(A + B) - CIN
V _L V _L V _H V _L	(A + B) - CIN
V _L V _L V _L V _H	A - CIN
V _L V _L V _L V _L	A

SCHEMATIC DIAGRAM
FOR
INSTRUCTION EXECUTION
LOGIC/A CIRCUIT CARD

TELETYPE
4400SD-6

ISSUE
1

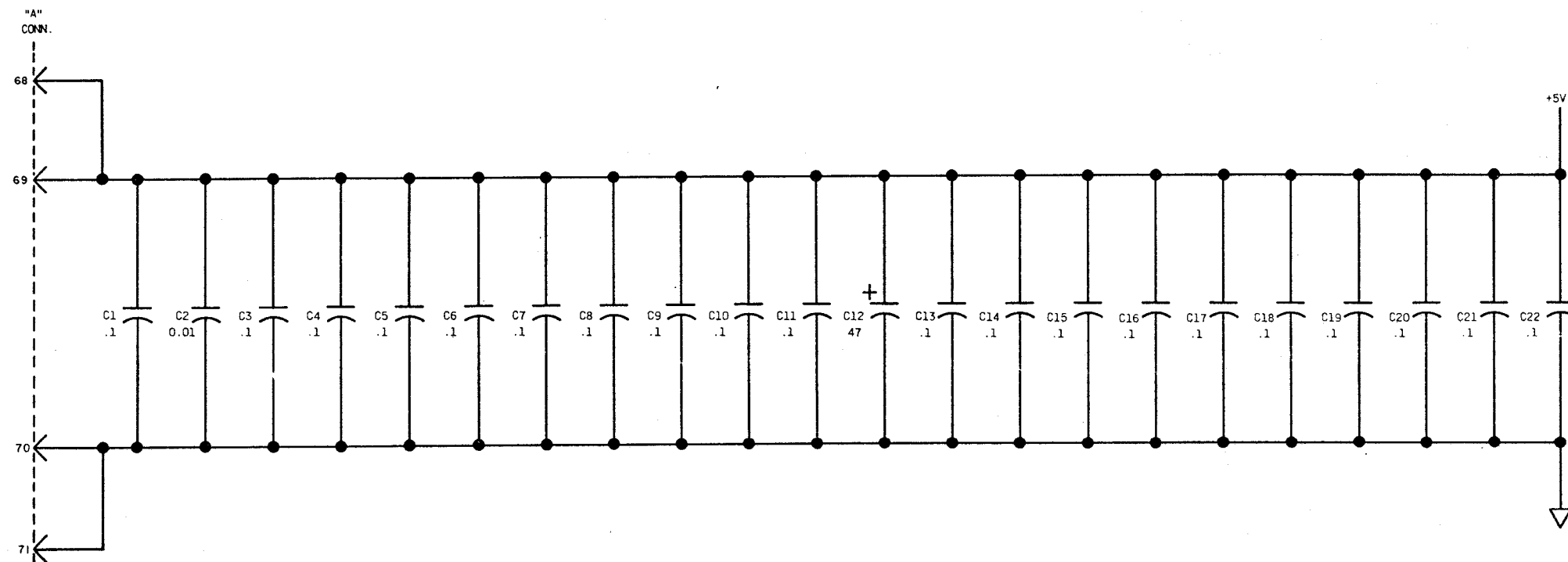


TELETYPE


48

FS - 6 POWER AND FILTER CIRCUITS

ISSUE
1

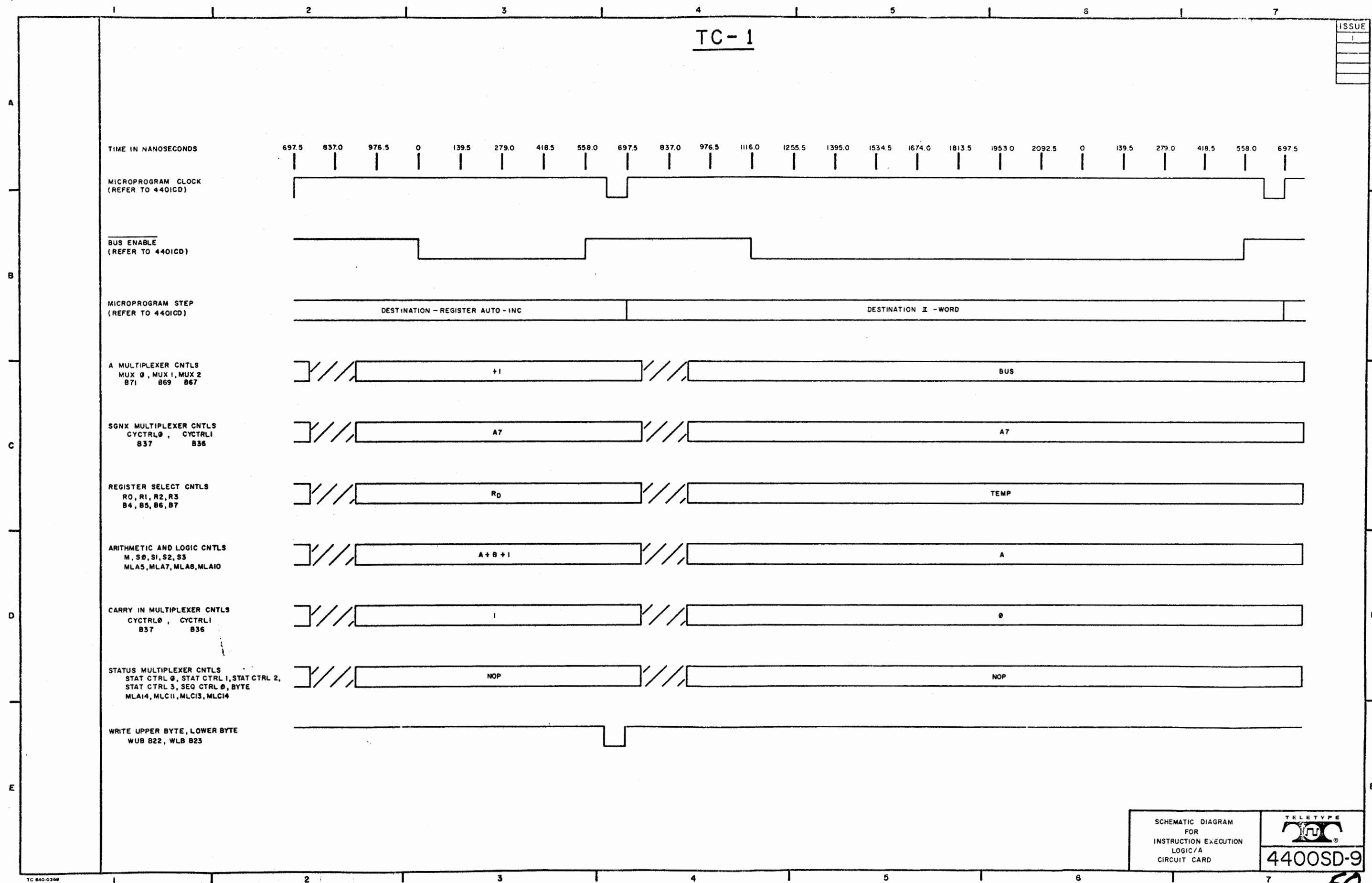


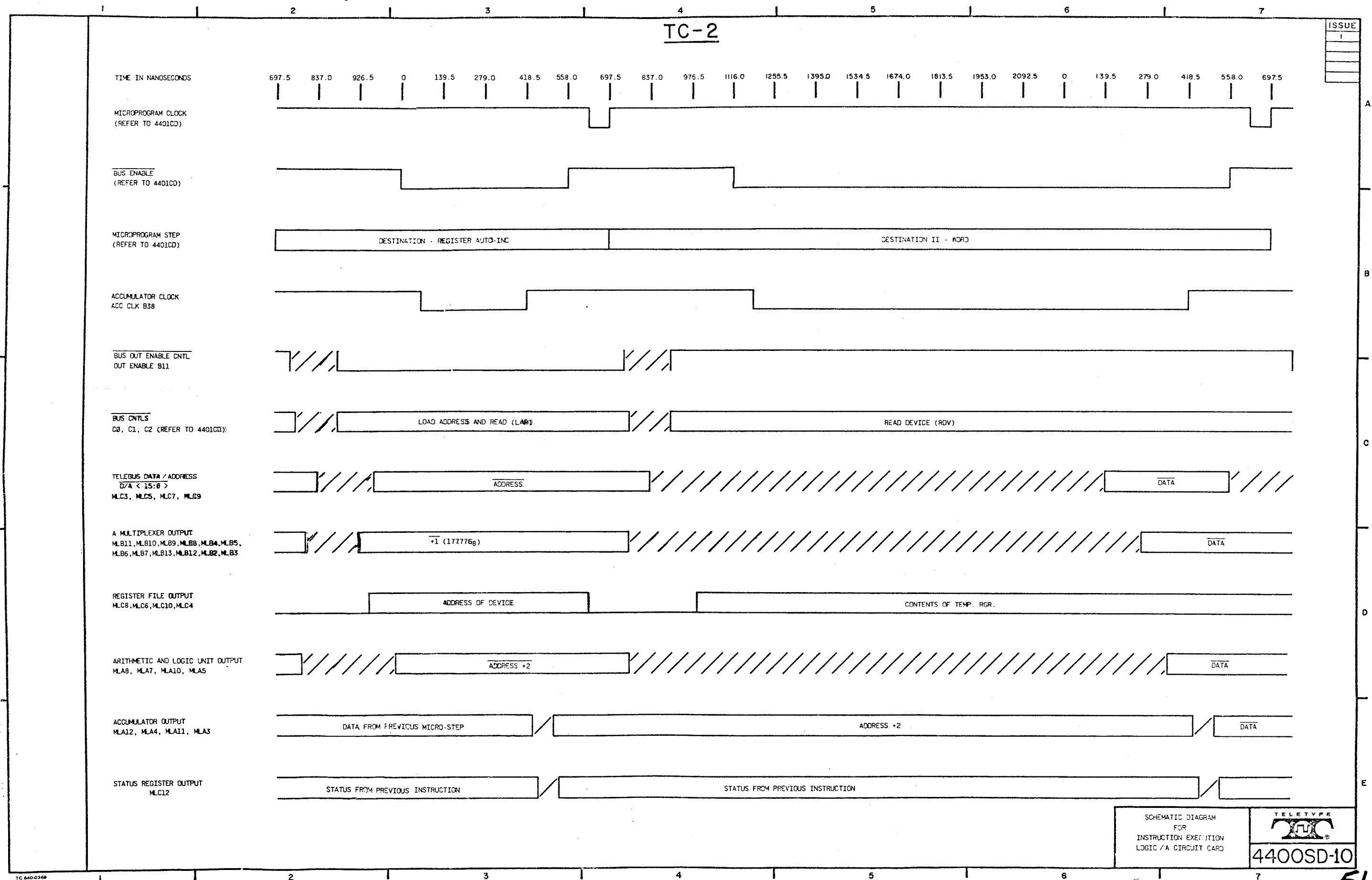
SCHEMATIC DIAGRAM
FOR
INSTRUCTION EXECUTION
LOGIC /A CIRCUIT CARD

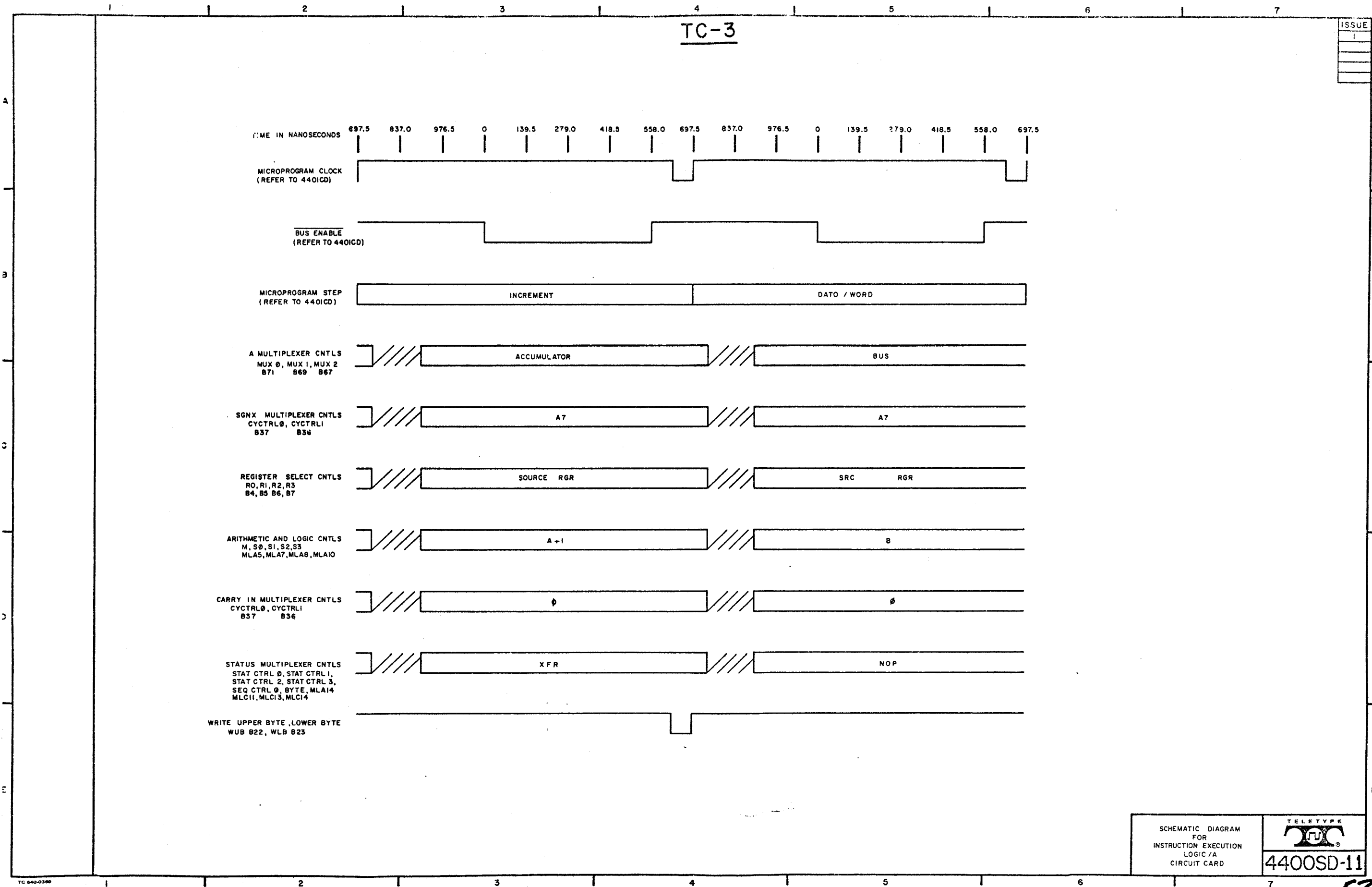


4400SD-8

49







TC-4

ISSUE
1

TIME IN NANSECONDS

697.5 837.0 976.5 0 139.5 279.0 418.5 558.0 697.5 837.0 976.5 0 139.5 279.0 418.5 558.0 697.5

MICROPROGRAM CLOCK
(REFER TO 4401CD)

BUS ENABLE
(REFER TO 4401CD)

MICROPROGRAM STEP
(REFER TO 4401CD)

ACCUMULATOR CLOCK
ACC CLK 838

BUS OUT ENABLE CNTL
OUT ENABLE BII

BUS CNTLS
C0, C1, C2 (REFER TO 4401CD)

TELEBUS DATA / ADDRESS
D/A 15:0
MLC3, MLC5, MLC7, MLC9

A MULTIPLEXER OUTPUT
MLB11, MLB10, MLB9, MLB8, MLB4, MLB5
MLB6, MLB7, MLB13, MLB2, MLB3

REGISTER FILE OUTPUT
MLC8, MLC6, MLC10, MLC4

ARITHMETIC AND LOGIC UNIT OUTPUT
MLA8, MLA7, MLA10, MLA5

ACCUMULATOR OUTPUT
MLA12, MLA4, MLA11, MLA3

STATUS REGISTER OUTPUT
MLC12

INCREMENT

DATO / WORD

NOP

WRITE

DATA +1

DATA

DATA +1

CONTENTS OF SOURCE RGR

DATA +1

DATA +1

DATA +1

DATA

DATA +1

STATUS FROM PREVIOUS INSTRUCTION

NEW STATUS CALCULATED N, Z, C = 0

SCHEMATIC DIAGRAM
FOR
INSTRUCTION EXECUTION
LOGIC / A CIRCUIT CARD



4400SD-12

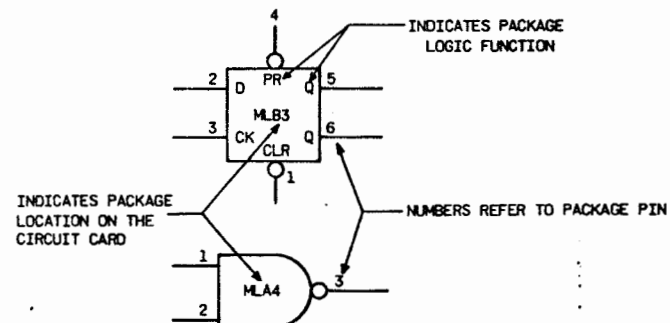
SHEET INDEX

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SHEET INDEX, SUPPORTING INFORMATION	1	1	2	3	4	5	6																				1
BLOCK DIAGRAM	2	1	1	1	1	1	1																				2
FS-1 MACRO INSTRUCTION REGISTER	3	1	1	1	1	1	1																				3
FS-2 INSTR. DECODE & MAJOR STATE CONTROL LOGIC	4	1	1	1	1	1	1																				4
FS-3 NEXT STATE ADDRESS ENCODING LOGIC	5	1	1	1	2	2	3																				5
MAJOR STATE AND ADDRESS ENCODING TABLES	6	1	1	1	1	1	1																				6
FS-4 MICRO-PROGRAM ADDRESSING LOGIC AND MICRO-PROGRAM STORAGE ARRAY NO. 1	7	1	1	1	1	1	1																				7
FS-5 MICRO-PROGRAM STORAGE ARRAY NO. 2 AND REGISTER FILE ADDRESSING LOGIC	8	1	1	1	1	1	1																				8
MICRO-PROGRAM CONTROL FIELD CODING	9	1	1	1	1	1	1																				9
FS-6 BUS CONTROL, INTERRUPT, AND SELF TEST LOGIC	10	1	2	3	3	4	4																				10
TC-1 NOMINAL TIMING DIAGRAM	11	1	1	1	1	1	1																				11
TC-2 RDV TIMING DIAGRAM	12	1	1	1	1	1	1																				12
TC-3 TIMING DIAGRAM FOR STANDBY POWER OPERATION	13	1	1	1	1	1	1																				13
TC-4 MICRO-PROGRAM TIMING DIAGRAM	14	1	1	1	1	1	1																				14
TC-5 MICRO-PROGRAM, INTERRUPT TIMING DIAGRAM	15	1	1	1	1	1	1																				15
FS-8 POWER AND FILTER CIRCUITS	16	1	1	1	1	1	1																				16

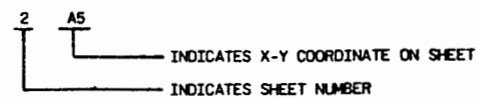
NOTES:

1. THE VOLTAGE, +5V, IS APPLIED TO PIN 8 OF THE 8 PIN PACKAGE, PIN 14 OF 14 PIN PACKAGES, PIN 16 OF 16 PIN PACKAGES, AND PIN 24 OF 24 PIN PACKAGES. GROUND IS APPLIED TO PIN 4 OF THE 8 PIN PACKAGE, PIN 7 OF 14 PIN PACKAGES, PIN 8 OF 16 PIN PACKAGES, AND PIN 12 OF 24 PIN PACKAGES.

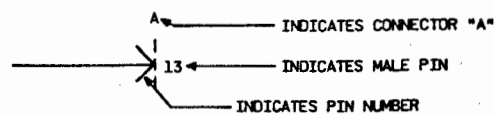
2. LOGIC NOTATION



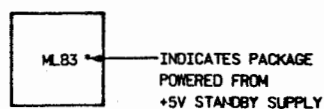
3. SHEET LOCATION CODE



4. CONNECTOR CODE



5. +5 VOLT STANDBY CODE



6. ALL CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

7. CONNECTOR PIN ASSIGNMENT

CONNECTOR	PIN	DESCRIPTION	SHEET LOCATION
A	8	INTG (OUT)	9D2
A	10	INTR	9D3
A	11	DEV A ENABLE	9D4
A	12	DEV B ENABLE	9D3
A	15	INITIALIZE	9D3
A	17	TRAP	9D3
A	19	C0	9D2
A	20	C1	9D2
A	21	C2	9D2
A	1	I/O CLK	10D7
A	3	BUS EN	10B7
A	5	MEM CLK	10B7

CONNECTOR	PIN	DESCRIPTION	SHEET LOCATION
B	1	LOAD	3
B	2	OSC EN	10D1
B	3	MUX EN	10D1
B	4	R2	7E4
B	5	R3	7E4
B	6	R1	7E5
B	7	R0	7E5
B	8	D/A (0)	3A6
B	9	BYTE	3E2
B	10	D/A (1)	3A6
B	11	OUT ENABLE	6E4
B	12	D/A (2)	3A6
B	13	D/A (3)	3A6
B	14	D/A (4)	3A6
B	15	D/A (5)	3A5
B	16	D/A (6)	3A4
B	17	D/A (7)	3A4
B	20	D/A (8)	3A4
B	22	MUB	7E6
B	23	MLB	7E6
B	24	D/A (9)	3A4
B	25	D/A (10)	3A4
B	26	D/A (11)	3A4
B	27	D/A (12)	3A3
B	28	D/A (13)	3A2
B	29	D/A (14)	3A2
B	30	D/A (15)	3A2

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT DESCRIPTION	4400CD
SCHEMATIC DIAGRAMS	4400SD
CIRCUIT DESCRIPTION	4401CD

USE OF SHEET INDEX

WHEN CHANGES ARE MADE IN THIS DRAWING

1. ONLY CHANGED SHEETS WILL BE REISSUED, INCLUDING SHEET 1.
2. UNCHANGED SHEETS RETAIN EXISTING ISSUE NUMBER.

THE LAST COMPLETED COLUMN ON THE SHEET INDEX INDICATES THE LATEST ISSUE PER SHEET.

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	3-13-75	23862R
2	2-16-76	16055
3	4-2-76	11684
4	12-20-76	18006
5	2-9-77	18078
6	5-22-77	18583

CONNECTOR	PIN	DESCRIPTION	SHEET LOCATION
B	31	STAT CTRL 3	6E5
B	32	STAT CTRL 2	6E5
B	33	STAT CTRL 1	6E5
B	34	STAT CTRL 0	6E5
B	35	CNTEN	6B6
B	36	CY CTRL 1	6E6
B	37	CY CTRL 0	6E6
B	38	ACC CLK	10B7
B	39	SEQ CTRL 0	6E7
B	43	M	7C3
B	47	Z	3D6
B	48	P	4E1
B	49	C	3D6
B	52	T	4E1
B	54	INTR	9D6
B	55	RESTART	10E1
B	57	N	3D6
B	58	MPS 0	7C4
B	59	MPS 1	7C4
B	60	MPS 2	7C4
B	61	MPS 3	7C4
B	63	MUX SEL 4	7C6
B	65	MUX SEL 3	7C7
B	67	MUX SEL 2	7C7
B	69	MUX SEL 1	7C7
B	70	RUN (IN)	9E5
B	71	MUX SEL 0	7C7

8. ALL RESISTANCE VALUES IN OHMS UNLESS OTHERWISE SPECIFIED.

9. VOLTAGE LEVELS:
L = 0V TO +0.4V
H = +2.4V TO +5.5V

10. LOGIC SYMBOLS
V = LOGIC OR
A = LOGIC AND
+ = LOGIC EXCLUSIVE OR

11. TIMING CHARTS
///// = INDETERMINATE
NOT LOGIC 1 OR LOGIC 0.

SCHEMATIC DIAGRAM
FOR
INSTRUCTION
EXECUTION
LOGIC/B
CARD ASSEMBLY

APPROVALS

PROJ. SUPV.	PROJ. ENGR.	MFG. REL. COMPL.
ENGR. S.A.	DSGMR.	
DRN. M.H.H.	DATE	
R&D FILE	6-167.172AA	
S-NUMBER	4401	

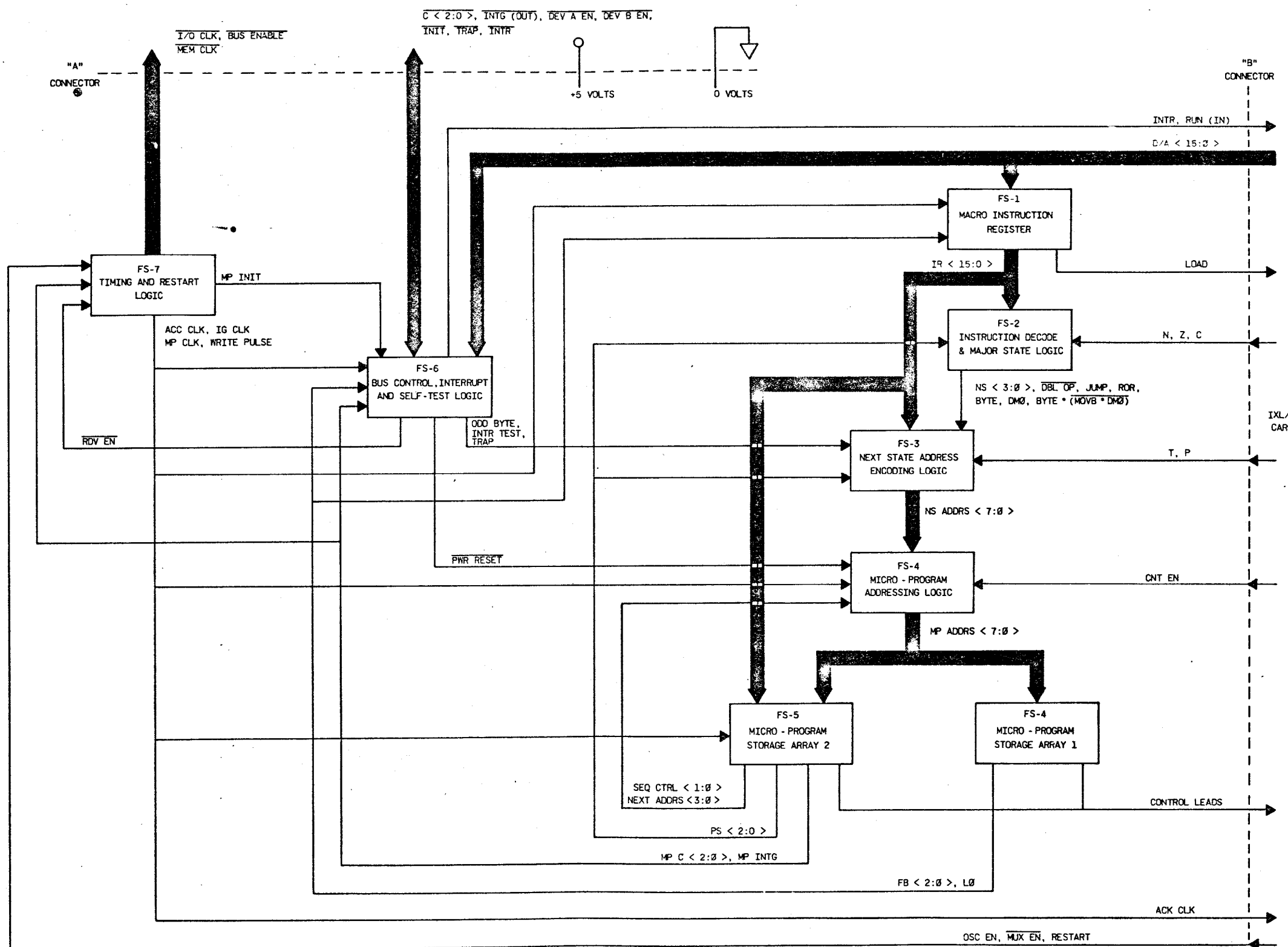
TELETYPE



4401SD-1

BLOCK DIAGRAM

ISSUE
1

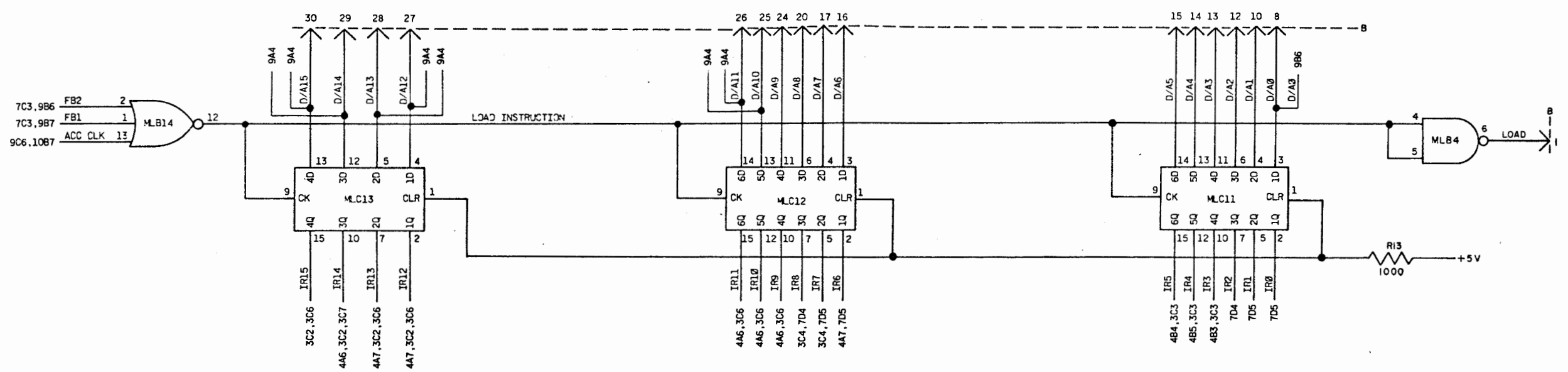


SCHEMATIC DIAGRAM
FOR
INSTRUCTION EXECUTION
LOGIC / B CARD ASSEMBLY

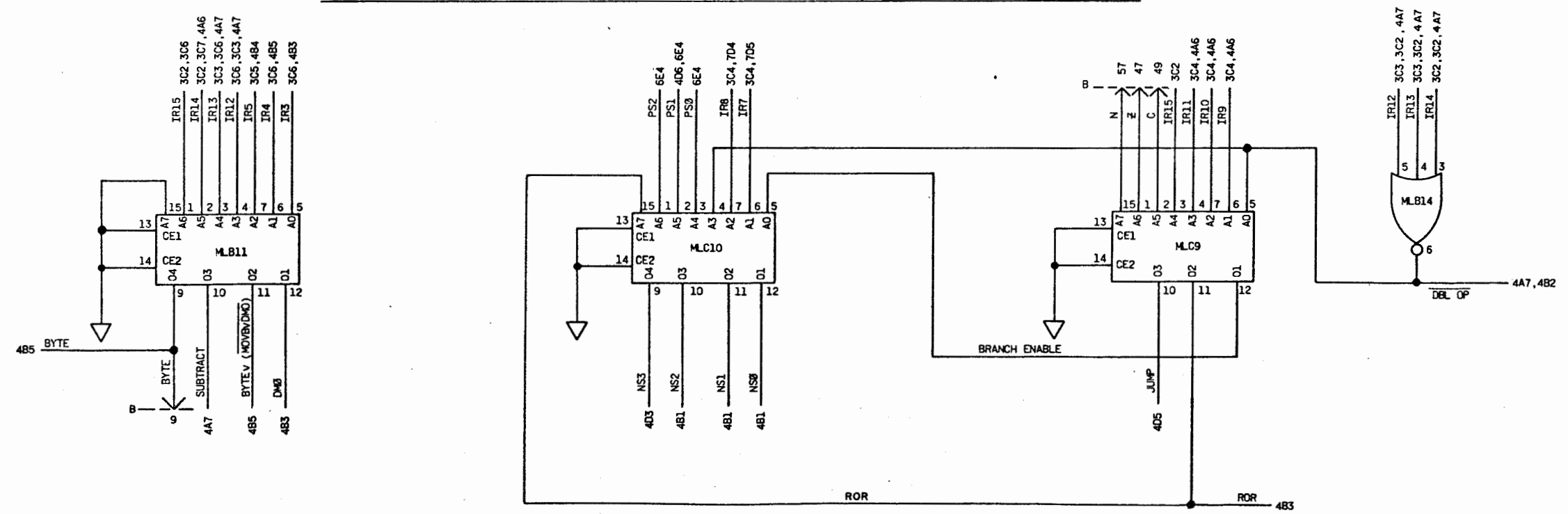


4401SD-2

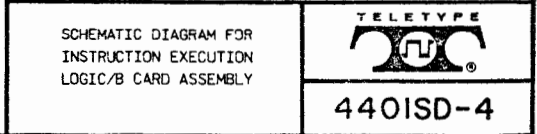
FS-1 MACRO INSTRUCTION REGISTER



FS-2 INSTRUCTION DECODE AND MAJOR STATE CONTROL LOGIC



ISSUE
1



NEXT MAJOR STATE TRANSITION TABLE

MICRO - PROGRAM ADDRESS FIELDS (OCTAL)	PRESENT STATE		INSTRUCTION TYPE				NEXT STATE			
	NAME	PS2, PS1, PS0	NAME	IR7, IR8, DBL OP, ROR, BREN			NAME	NS3, NS2, NS1, NS0		
0-37	FETCH	L L L	BRANCH (NOT ENABLED) BRANCH (ENABLED) CONTROL GROUP DOUBLE OPERAND GROUP SINGLE OPERAND GROUP	X H L X L X H L X H L L L X X X X H X X H L L X X			FETCH BRANCH CONTROL SOURCE DESTINATION	L H L L H H H H L L L L L H L H H H H L		
40-43	SOURCE A (SEE NOTE 1)	L H L					DESTINATION	H H H L		
44-77	SOURCE B (SEE NOTE 1)	L L H					SOURCE II	H L H H		
102-103	DESTINATION A (SEE NOTE 1)	H L L	NOT ROR ROR	X X X L X X X X H X			EXECUTE DESTINATION II	H L L H H L H H		
100-101, 104-137	DESTINATION B (NOTE 1)	L H H					DESTINATION II	H L H H		
140-141, 144-177	DESTINATION C (NOTE 1)	H L H					EXECUTE	H L L H		
142-143	BRANCH	H H H					FETCH	L H L L		
200-307, 320-327	CONTROL	H H H					FETCH	L H L L		
310-317	SOURCE II	L H L					DESTINATION	H H H L		
320-337	DESTINATION II	H L H					EXECUTE	H L L H		
(NOTE 3)	EXECUTE B (NOTE 1)	H H L					DATO	H L H L		
(NOTE 4)	EXECUTE A (NOTE 1)	H H H					FETCH	L H L L		
360-367	DATO	H H H					FETCH	L H L L		

NOTES:

- SOURCE A FIELD DEFINES MODE 0
SOURCE B FIELD DEFINES MODES 1 THRU 7
DESTINATION A FIELD DEFINES MODE 0 BYTE
DESTINATION B FIELD DEFINES MODES 1 THRU 7 AND MODE 0 WORD
DESTINATION C FIELD DEFINES THE JUMP MODES
EXECUTE A FIELD DEFINES THE INSTRUCTIONS BIT, CMP, TST, JAP AND JSR

EXECUTE B FIELD DEFINES ALL OTHER SINGLE OP OR DOUBLE OP INSTRUCTION
NOT IN EXECUTE A.

- 'H' DENOTES A HIGH LOGIC LEVEL
'L' DENOTES A LOW LOGIC LEVEL.
'X' DENOTES DON'T CARE

- 340, 341, 344-353, 355-360, 362-364, 366, 370-375.
- 342, 343, 354, 361, 365, 367, 376, 377.

NEXT STATE ADDRESS ENCODING TABLE

NEXT STATE		NEXT MICRO-ROUTINE ADDRESS							
NAME	NS3, NS2, NS1, NS0	A7	A6	A5	A4	A3	A2	A1	A0
FETCH	L H L L	L	L	L	TEST	TRAP $\wedge$ TEST	A (SEE NOTE 1)	B (SEE NOTE 1)	L
SOURCE	L H L H	L	L	H	IR11	IR10	IR9	BYTE	L
SOURCE II	H L H H	H	H	L	L	H	L	BYTE	000 BYTE
DESTINATION	H H H L	L	H	JUMP	IR5	IR4	IR3	BYTE	L
DESTINATION II	H L H H	H	H	L	H	H	ROR	BYTE	000 BYTE
EXECUTE	H L L H	H	H	H	DBL OP $\wedge$ IR11	DBL OP	C (SEE NOTE 1)	D (SEE NOTE 1)	E (SEE NOTE 1)
CONTROL	L L L L	H	IR11	IR10	IR9	IR6	IR5	IR4	L
BRANCH	H H H H	L	H	H	L	L	L	H	L
DATO	H L H L	H	H	H	H	L	DM0	BYTE $\wedge$ (MOV + DM0)	000 BYTE

NOTES:

- $A = INTR \wedge \overline{T} \wedge \overline{P} \wedge \overline{TEST} \wedge \overline{TRAP}$
 $B = (\overline{INTR} \vee T \vee P) \wedge \overline{TEST} \wedge \overline{TRAP}$
 $C = DBL\ OP \wedge IR14 \wedge SUB \vee DBL\ OP \wedge IR10$
 $D = DBL\ OP \wedge IR13 \wedge SUB \vee DBL\ OP \wedge IR9$
 $E = DBL\ OP \wedge IR12 \wedge SUB \vee DBL\ OP \wedge IR6$

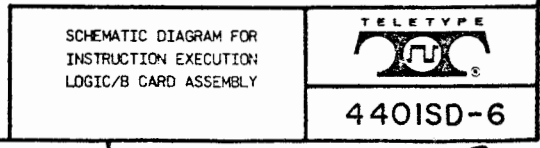
- 'H' DENOTES A HIGH LOGIC LEVEL
'L' DENOTES A LOW LOGIC LEVEL

SCHEMATIC DIAGRAM FOR
INSTRUCTION EXECUTION
LOGIC/B CARD ASSEMBLY



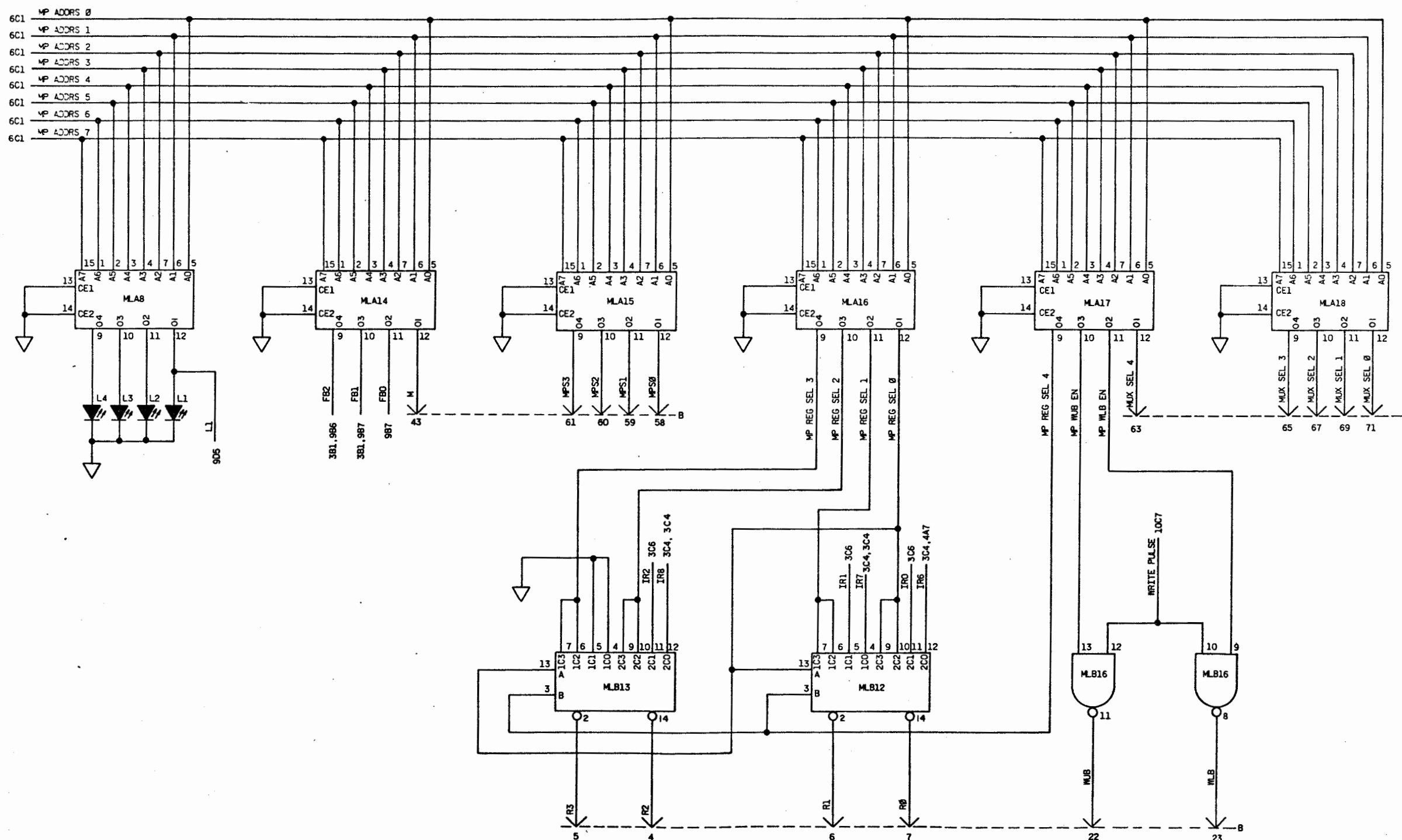
440ISD-5

ISSUE
1



FS-5 MICRO-PROGRAM STORAGE ARRAY NO. 2 AND REGISTER FILE ADDRESSING LOGIC

ISSUE
1-



SCHEMATIC DIAGRAM FOR
INSTRUCTION EXECUTION
LOGIC / B CARD ASSEMBLY

TELETYPE
4401SD-7

MICRO-PROGRAM CONTROL FIELD CODING

"A" MULTIPLEXER CONTROL

MUX SEL 4 MUX SEL 3 MUX SEL 2 MUX SEL 1 MUX SEL 0	FUNCTION
L L L L L	BUS
L H L L L	BUS SGNX
L H L L H	BUS SWAB SGNX
L L H L L	ACC
L H H L L	ACC SGNX
H L H L L	ACC SWAB
H H H L L	ACC - SR
L H H H H	STATUS
L H L H L	+1
L H L H H	-2

CARRY CONTROL

CYCTRL 1	CYCTRL 0	CIN	SGNX
L	L	0	A7
L	H	1	A7
H	L	CSTAT	A7
H	H	ACC 15	CSTAT

REGISTER SELECT

MP REG SEL 4 MP REG SEL 3 MP REG SEL 2 MP REG SEL 1 MP REG SEL 0	REGISTER
L L L L L	RS
L L L L H	RD
H L L L L	R0
H L L L H	R1
H L L H L	R2
H L L H H	R3
H L H L L	R4
H L H L H	R5
H L H H L	R6
H L H H H	R7 (SP)
H H L L L	PC
H H L L H	SRC
H H L H L	TEMP
H H L H H	X
H H H L L	Y
H H H L H	Z
H H H H L	IV
H H H H H	TRAP

ALU CONTROL

MPS 3 MPS 2 MPS 1 MPS 0	M=0 - ARITHMETIC OPER.	M=1 - LOGIC OPERATIONS
L L L L	$A + C_{IN}$	A
L L L H	$A + A \wedge B + C_{IN}$	$A \wedge \bar{B}$
L L H L	$A + A \wedge B + C_{IN}$	$A \wedge B$
L L H H	$A + A + C_{IN}$	0
L H L L	$(A \vee B) + C_{IN}$	$A \vee \bar{B}$
L H L H	$(A \wedge B) + (A \vee B) + C_{IN}$	$\bar{B}$
L H H L	$A - B - \bar{C}_{IN}$	$A \vee B$
L H H H	$A + (A \vee B) + C_{IN}$	$A \vee B$
H L L L	$(A \vee B) + C_{IN}$	$A \vee B$
H L L H	$A + B + C_{IN}$	$A \vee B$
H L H L	$(A \wedge B) + (A \vee B) + C_{IN}$	B
H L H H	$A + (A \vee B) + C_{IN}$	$\bar{A} \wedge B$
H H L L	$\bar{C}_{IN}$	1
H H L H	$(A \wedge B) - \bar{C}_{IN}$	$A \wedge B$
H H H L	$(A \wedge B) - \bar{C}_{IN}$	$\bar{A} \vee B$
H H H H	$A - \bar{C}_{IN}$	$\bar{A}$

OTHER REGISTER CONTROLS

MP MUB (HIGH IS ACTIVE)

MP MLB (HIGH IS ACTIVE)

STATUS CONTROL

STAT CTRL 3 STAT CTRL 2 STAT CTRL 1 STAT CTRL 0	FUNCTION
L L L L	XFR
L L L H	SUB
L H L L	NOP (RECIRCULATE)
L H H L	ADD
L H H H	SHR
H L H H	BUS
H H L L	CLEAR T
H H L H	SET T

TELEBUS CONTROL

MPC 2 MPC 1 MPC 0	FUNCTION
L L L	NOP
L L H	RDV
L H L	LAR
L H H	LAD
H L L	MWI
H L H	WBI
H H L	ROI
H H H	RDW

OTHER TELEBUS CONTROLS

MP INTG (HIGH IS ACTIVE)

OUT ENABLE (LOW IS ACTIVE)

SEQUENCE - CTRL

SEQ CTRL 1 SEQ CTRL 0	FUNCTION
H L	BR Z=0
H H	BR Z=1
L L	BR
L H	DONE

FEED - BACK CONTROL

FB2 FB1 FB0	FUNCTION
L L L	LOAD INSTRUCTION
L L H	(ILLEGAL)
L H L	ODD BYTE ENABLE
L H H	SET TRAP
H L L	NOP
H L H	CLEAR ODD BYTE
H H L	ODD BYTE ENABLE
H H H	CLEAR TRAP

OTHER CONTROLS

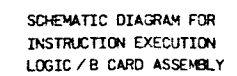
LED <0-3> (HIGH IS ACTIVE)

SCHEMATIC DIAGRAM
FOR
INSTRUCTION EXECUTION
LOGIC/B CARD ASSEMBLY

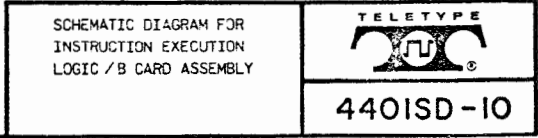


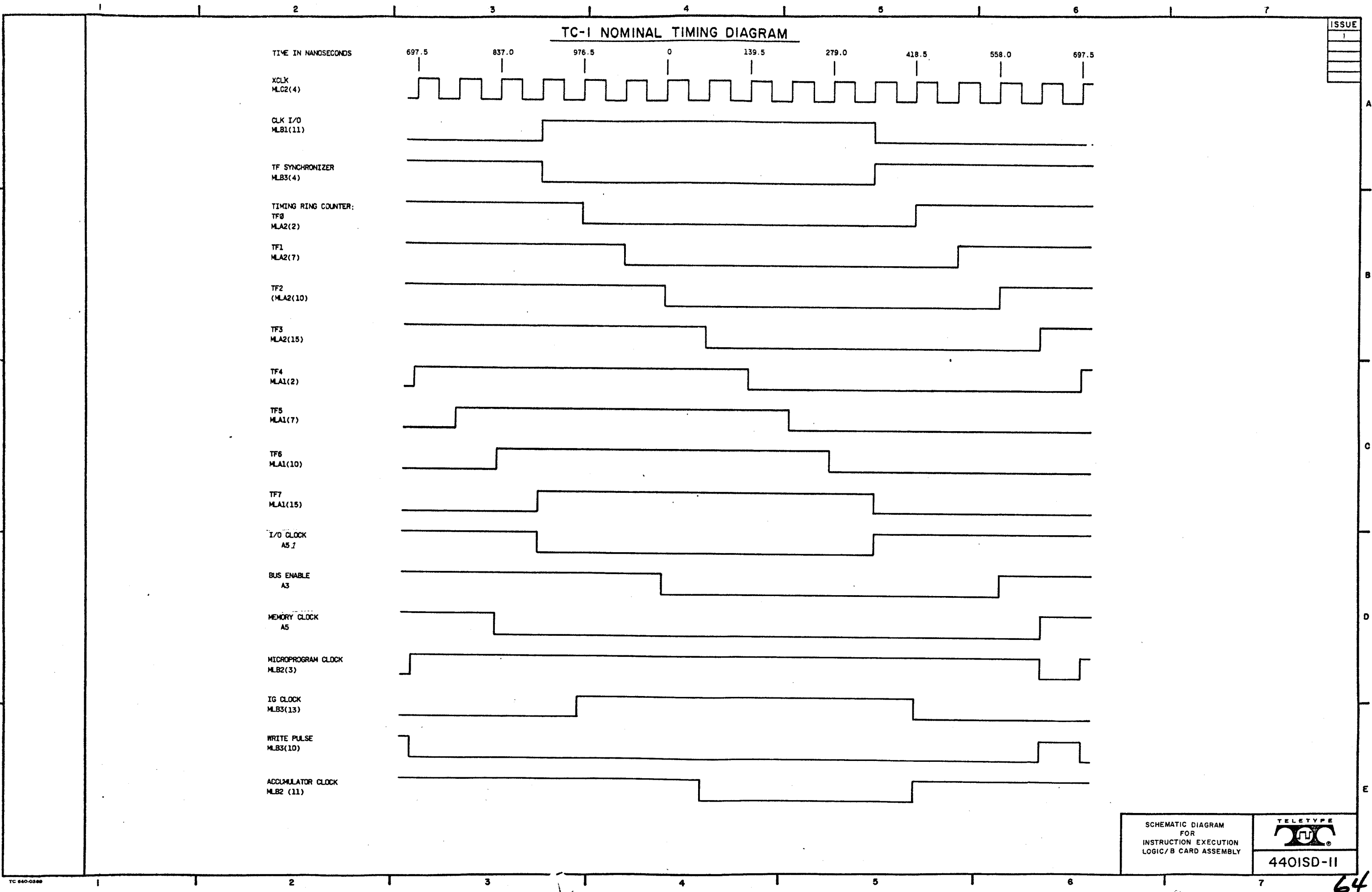
440ISD-8

ISSUE
1



4401SD-9





SCHEMATIC DIAGRAM
FOR
INSTRUCTION EXECUTION
LOGIC/B CARD ASSEMBLY

TELETYPE

440ISD-II

TC-2 RDV TIMING DIAGRAM

ISSUE
1

TIME IN NANSECONDS

XCLK
MLC2 (4)

CLK I/O
MLB1 (11)

XCLK CNTR CARRY
MLB1 (15)

TF SYNCHRONIZER
MLB3 (4)

TIMING RING CNTR OUTPUTS:
TF2
MLA2 (2)

TF3
MLA2 (15)

TF7
MLA1 (15)

RDV DECODE
MLA4 (12)

RDV EN
MLA4 (11)

RDV FF0
MLA3 (6)

RDV FF1
MLA3 (15)

MICROPROGRAM CLOCK
MLB2 (3)

ACCUMULATOR CLOCK
MLB2 (11)

I/O CLOCK
A1

BUS ENABLE
A3

MEMORY CLOCK
A5

SCHEMATIC DIAGRAM
FOR
INSTRUCTION EXECUTION
LOGIC/B CARD ASSEMBLY



440ISD-12

TC-3 TIMING DIAGRAM FOR STANDBY POWER OPERATION

ISSUE
1

TIME IN NANoseconds

POWER FAILURE INDICATION
MLA3 (10)

XCLK CNTR CARRY
MLB1 (15)

I/O CLK ENABLE
MLC4 (15)

I/O COUNTER LOAD
MLC4 (9)

MEMORY CLOCK
A5

I/O CLOCK
A1

BUS ENABLE
A3

2 THROUGH 15

17.856 mSEC

SCHEMATIC DIAGRAM
FOR
INSTRUCTION EXECUTION
LOGIC/B CARD ASSEMBLY



440ISD-13

TC-4 MICRO-PROGRAM TIMING DIAGRAM

TIME IN NANSECONDS

BUS ENABLE
A3

MP CLK
MLB2(3)

ACC CLK
MLB2(11)

LOAD INSTRUCTION
MLB14(12)

DATA/ADDRESS - D/A < 15:0 >
A25, A27, A29, A31, A33, A35, A37, A39,
A41, A43, A45, A47, A49, A51, A53, A55

MACRO INSTRUCTION REG
IR < 15:0 > MLC5, MLC11, MLC12, MLC13

NEXT STATE ADDRESS - NS ADDR < 7:0 >
MLB6, MLB7, MLB9, MLC6, MLC7, MLC8

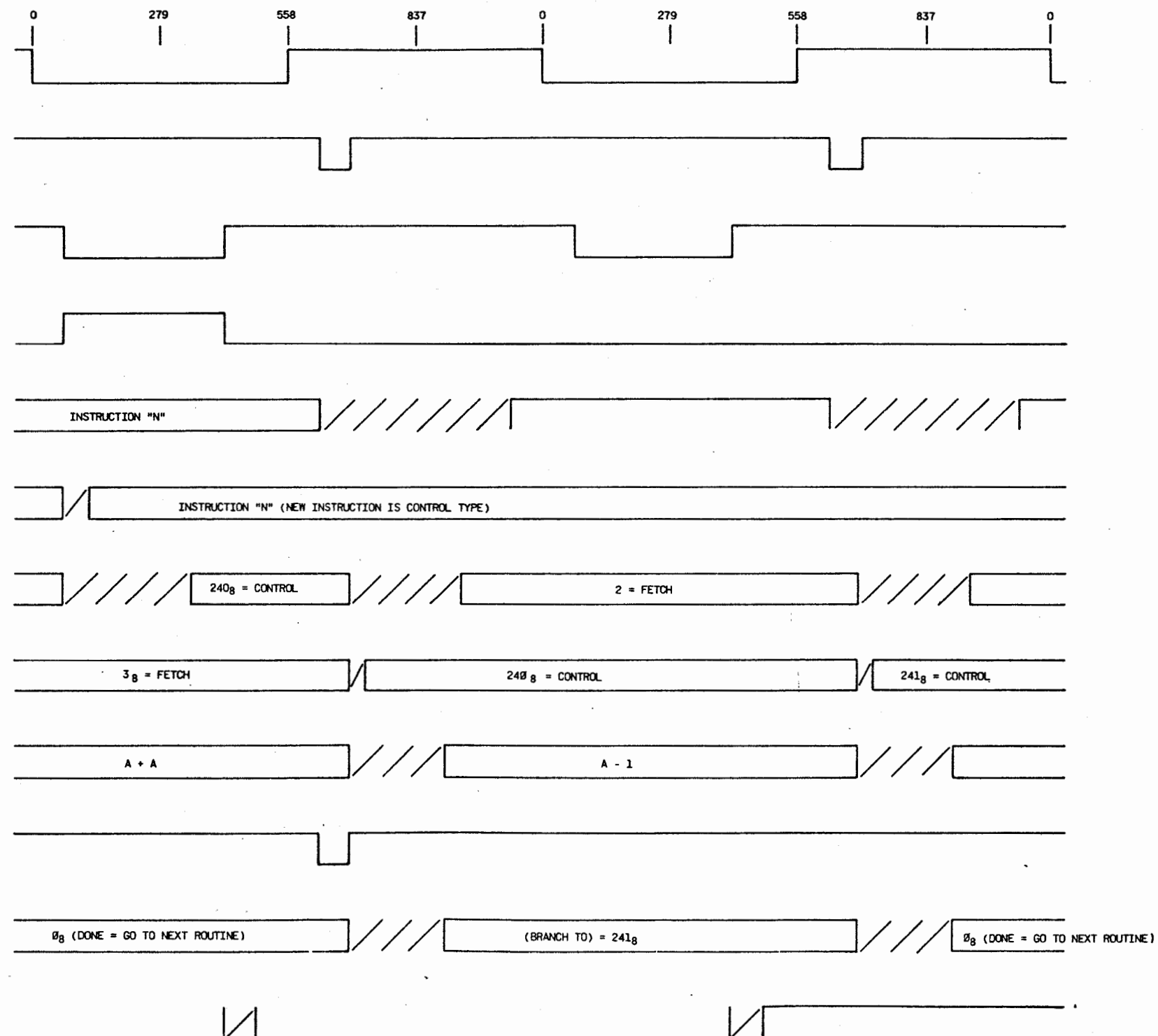
MP ADDRS < 7:0 >
MLA6, MLA7

MP STORAGE ARRAYS OUTPUTS:
ALU CONTROLS
MLA15, MLA14

WRITE UPPER BYTE, LOWER BYTE
MLB16(8), MLB16(11)

MP BRANCH ADDRESS MP BR ADDRS
MLA9 - SEQUENCE CONTROLS
SEQ CTRL < 0:1 > MLA13

CNT EN
B35



SCHEMATIC DIAGRAM
FOR
INSTRUCTION EXECUTION
LOGIC/B CARD ASSEMBLY



440ISD-14

TC-5 MICRO-PROGRAM INTERRUPT TIMING DIAGRAM

TIME IN NANoseconds

BUS ENABLE
A3

MP CLK
MLB2(3)

ACC CLK
MLB2(11)

DATA/ADDRESS - D/A < 15:0 >
A25, A27, A29, A31, A33, A35, A37, A39,
A41, A43, A45, A47, A49, A51, A53, A55

MACRO INSTRUCTION REGISTER
IR < 15:0 > MLC5, MLC11, MLC12, MLC13

NEXT STATE ADDRESS - NS ADDR < 7:0 >
MLB6, MLB7, MLB8, MLB9, MLC6, MLC7, MLC8

MP ADDRS < 7:0 >
MLA6, MLA7

MP STORAGE ARRAY OUTPUTS:
ALU CONTROLS
MLA15, MLA14

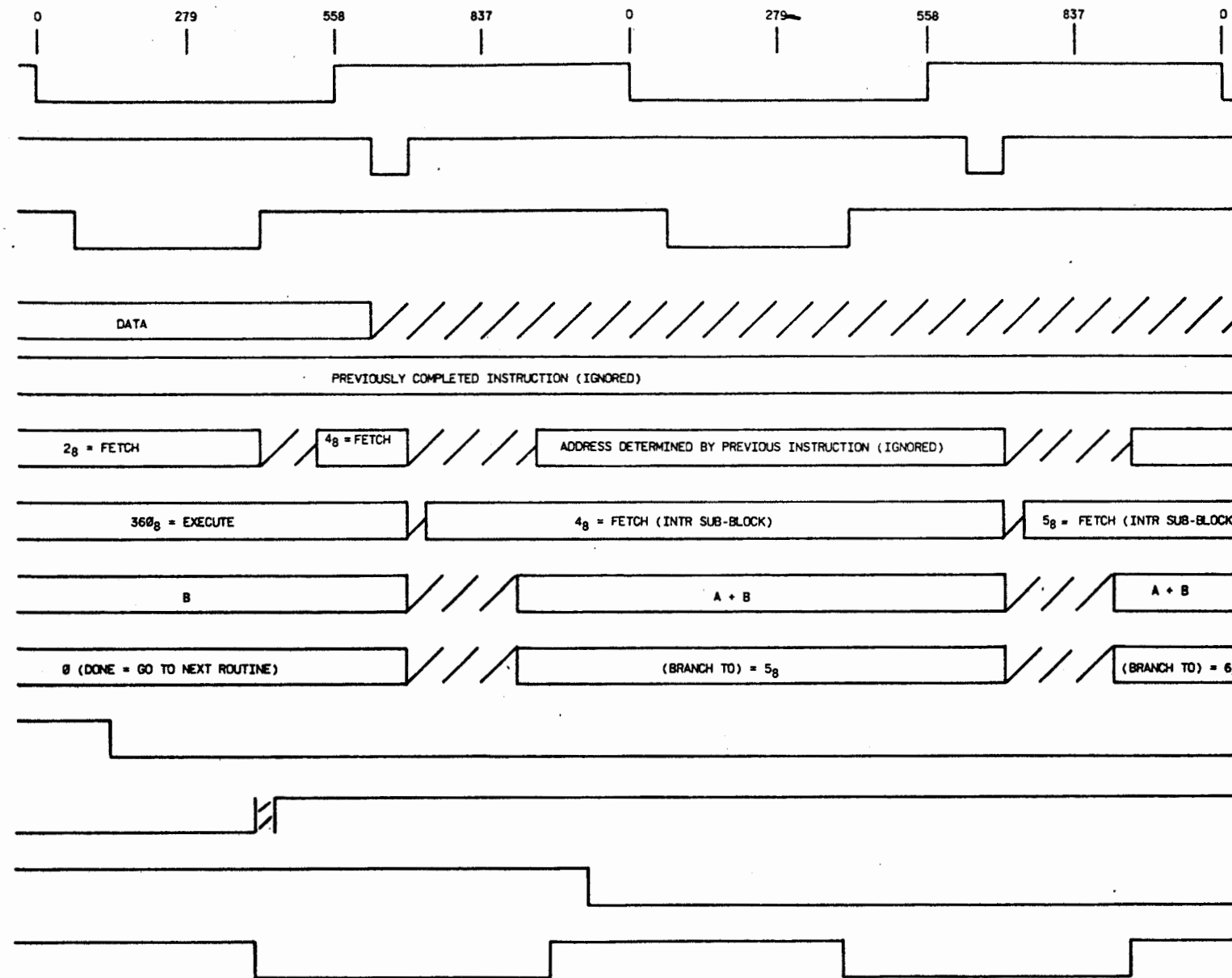
MP BRANCH ADDRESS (MP BR ADDRS)
MLA9 - SEQUENCE CONTROLS
SEQ CTRL < 1:0 > MLA13

TELEBUS INTR
A10

INTR
MLB(7)

TELEBUS INTG OUT OF IXL
A8

IG CLK
MLB3(13)

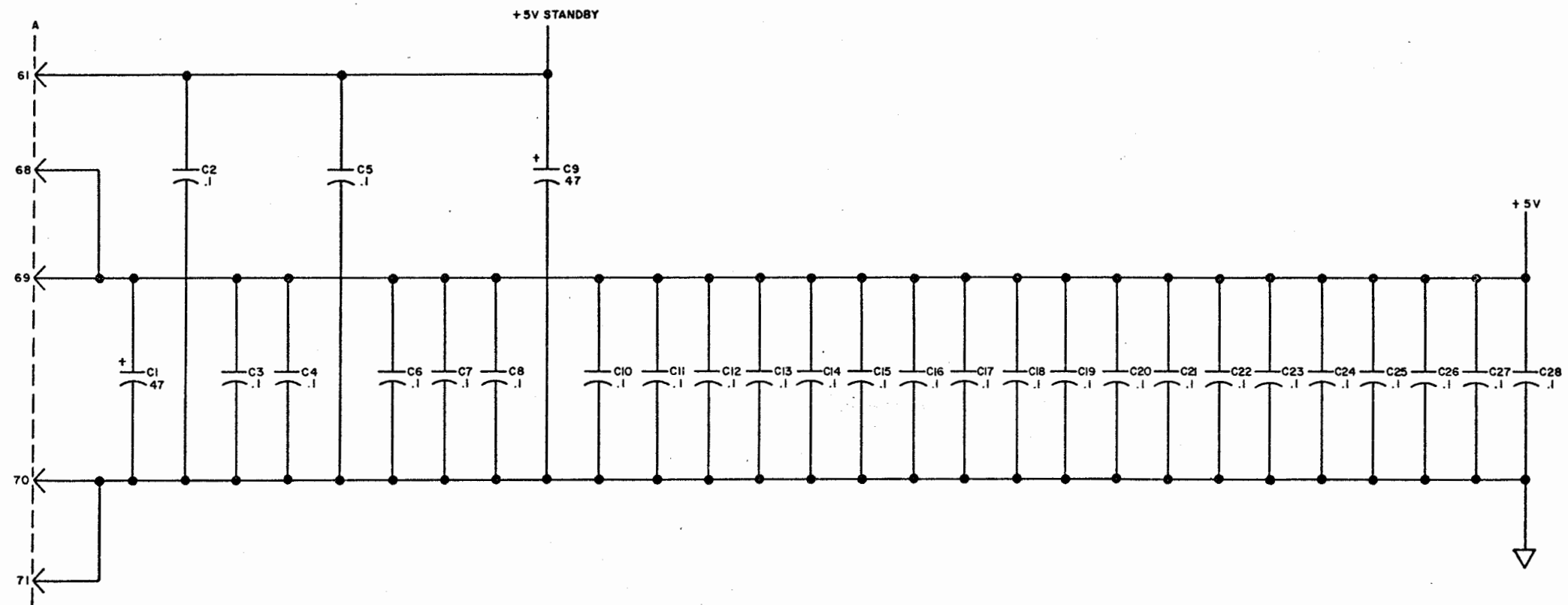


SCHEMATIC DIAGRAM FOR
INSTRUCTION EXECUTION
LOGIC/B CARD ASSEMBLY



4401SD-15

FS-8 POWER & FILTER CIRCUITS

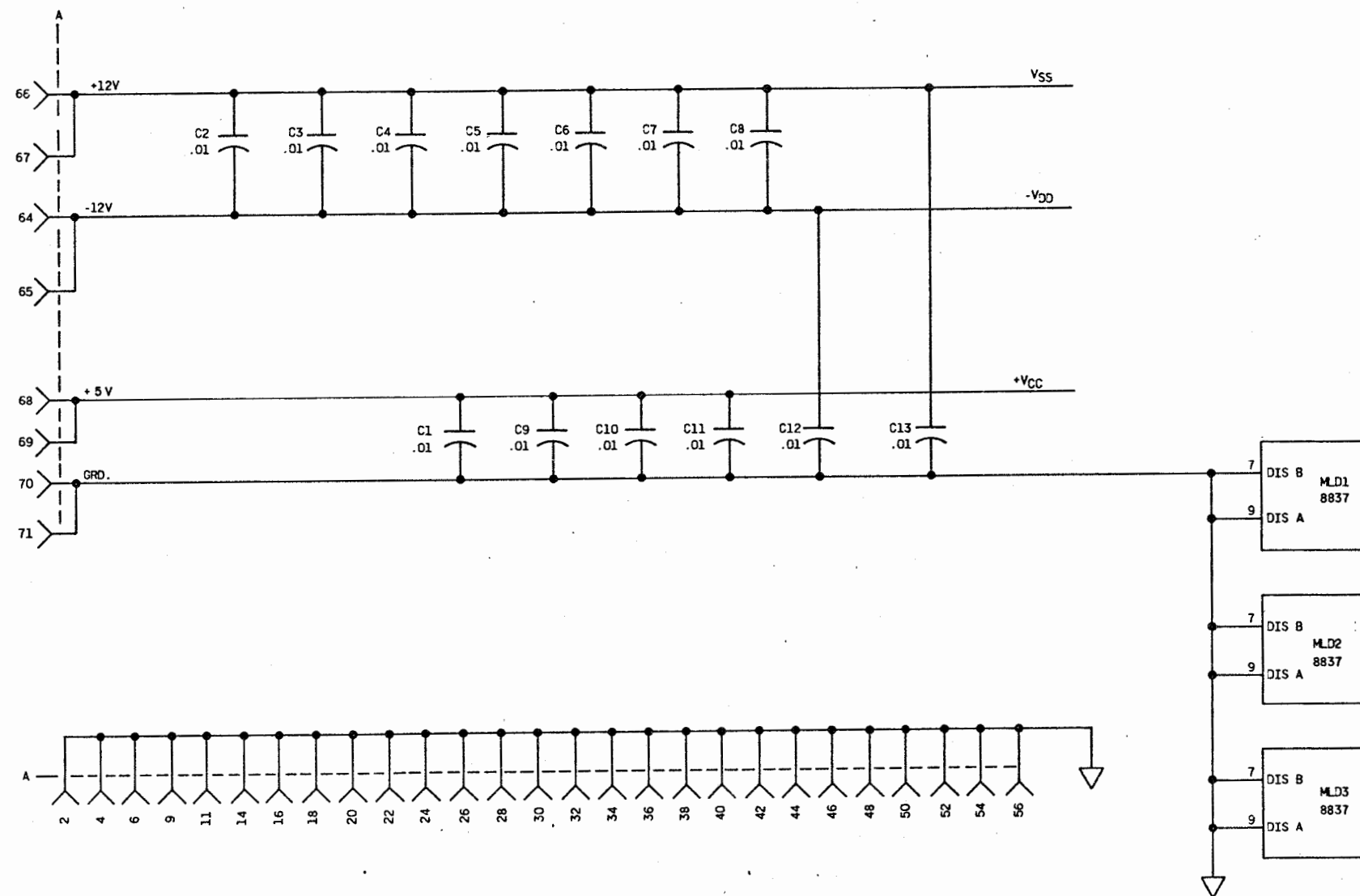


SCHEMATIC DIAGRAM
FOR
INSTRUCTION EXECUTION
LOGIC/B CARD ASSEMBLY



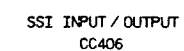
440ISD-16

FS-1
POWER DISTRIBUTION AND SHIELDING



NOTE: 2. ON CUSTOMER I. D. ISSUE 6C, THE VALUE OF R1 - R8 IS 10K.

ISSUE
- 1
2
3

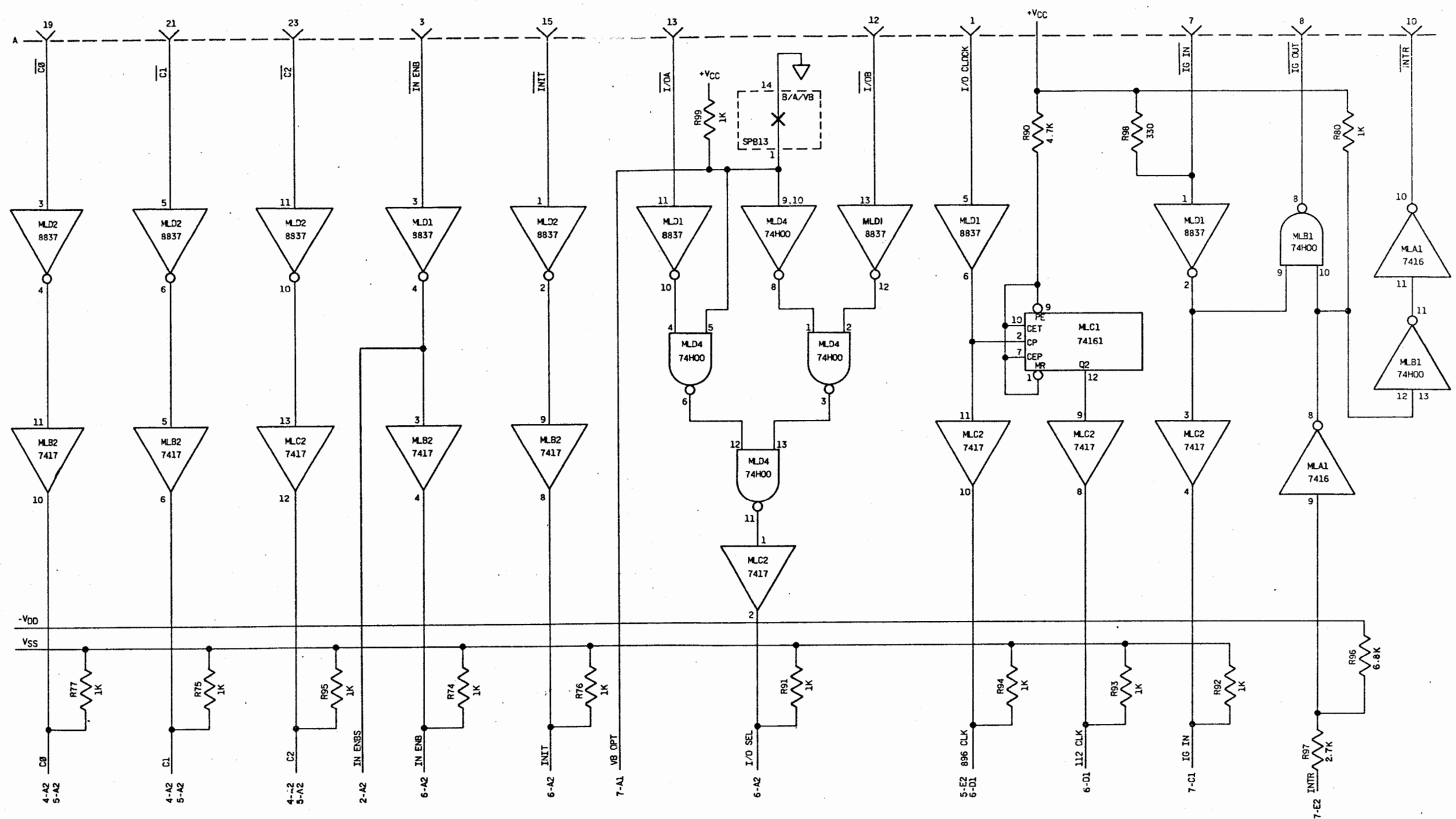


4406SD-B2

NOTE: 2. ON CUSTOMER I.D. ISSUE 6C, THE VALUE OF R96 IS 10K, AND ON ISSUE 6C AND LOWER, THE VALUE OF R97 IS 5.1K.

CONTROL AND INTERRUPT LOGIC LEVEL SHIFTING

ISSUE
1
2
3
4



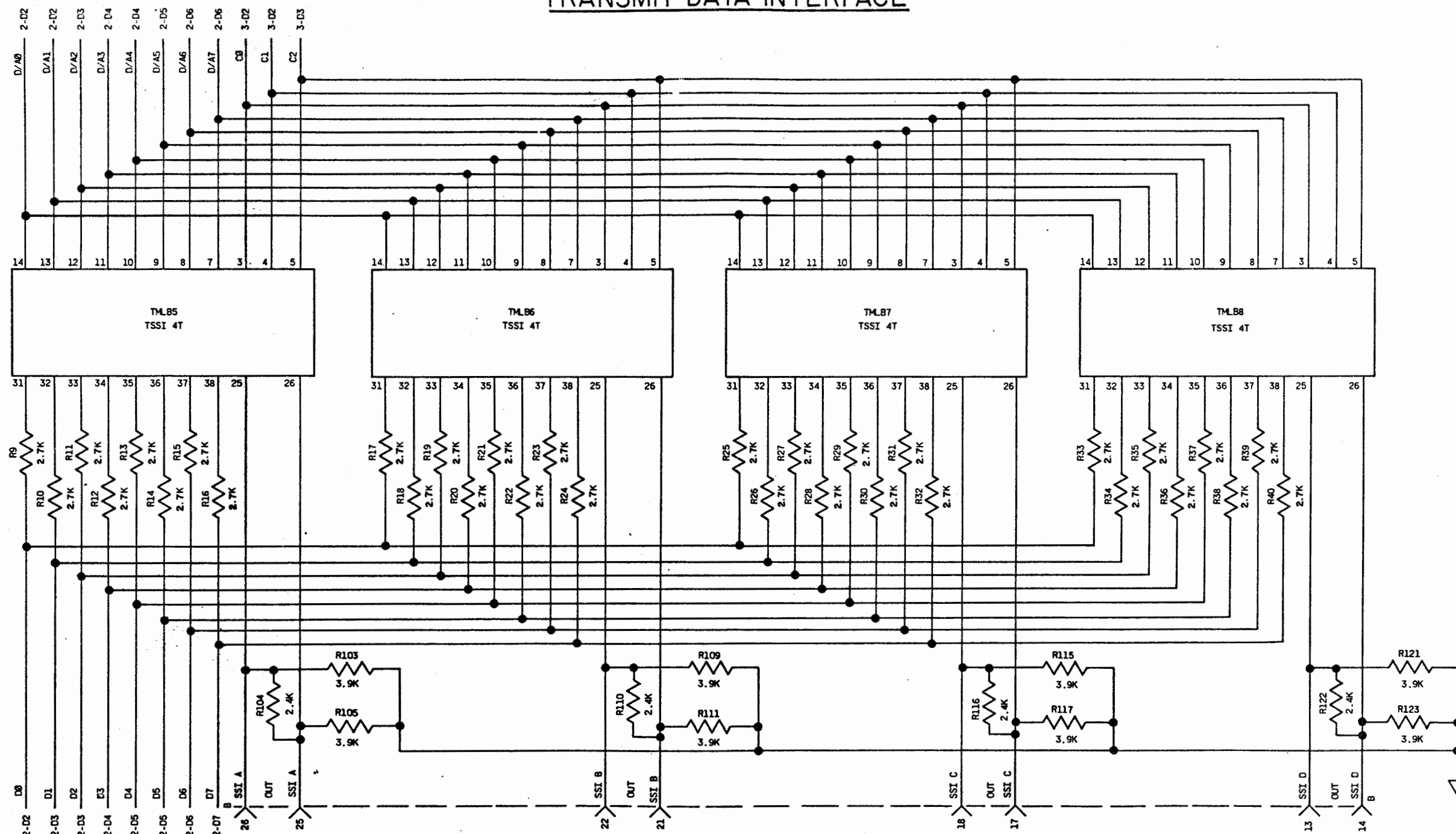
TELETYPE


4406SD-B3

FS-4 TRANSMIT DATA INTERFACE

NOTE: 1. ON CUSTOMER I. D. ISSUE 6C AND LOWER THE VALUE
OF R9-R40 IS 5.1K.

ISSUE
1
2



SSI INPUT / OUTPUT
CC406

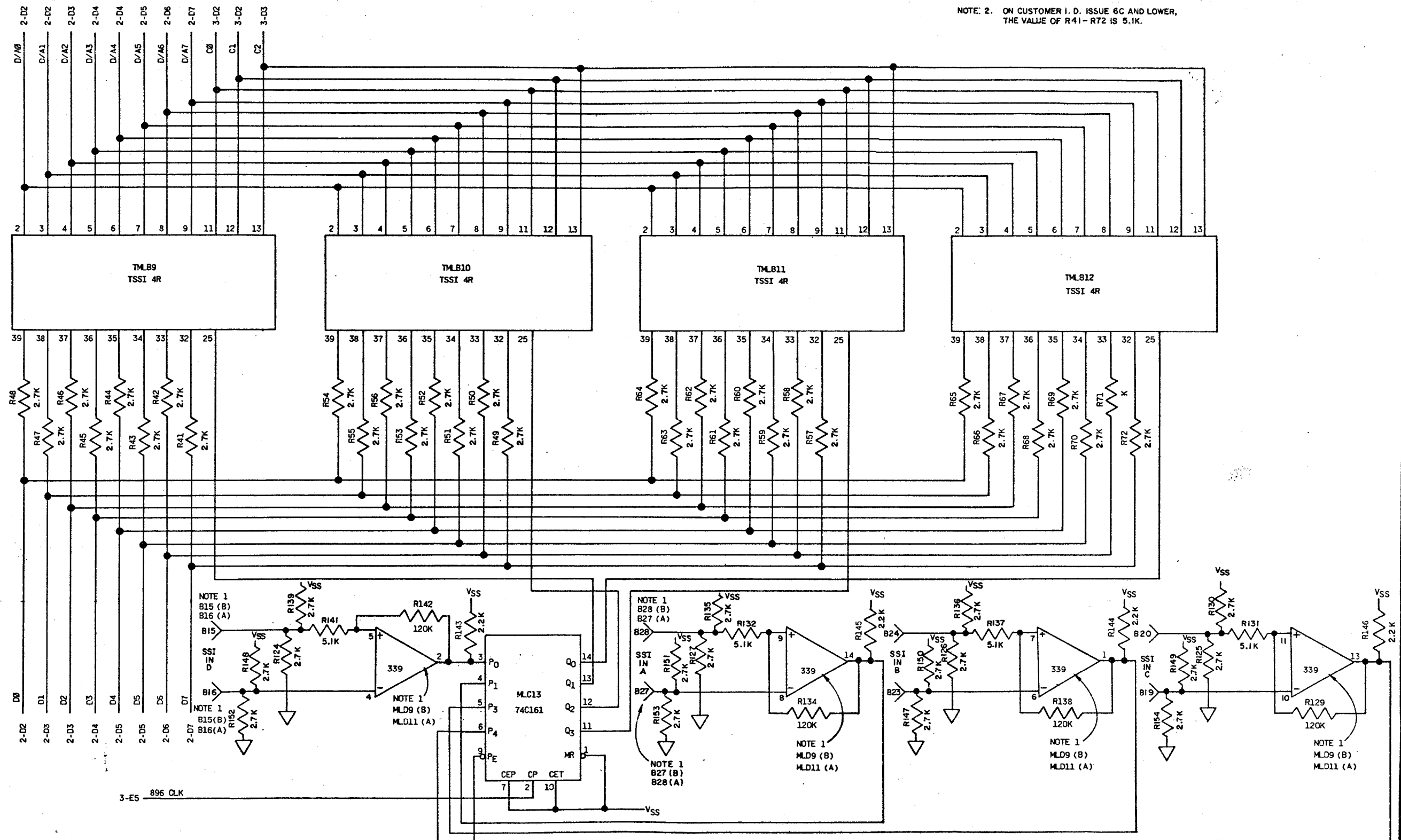


4406SD - B4

FS-5 RECEIVE DATA INTERFACE

NOTE 1. ON 409406 ISSUE 4A AND HIGHER
MLD9 IS RENAMED MLD11
INPUT B15 IS CONNECTED TO MLD11-4
INPUT B16 IS CONNECTED TO R141
INPUT B27 IS CONNECTED TO R132
INPUT B28 IS CONNECTED TO MLD11-8.

NOTE 2. ON CUSTOMER I. D. ISSUE 6C AND LOWER,
THE VALUE OF R41-R72 IS 5.1K.



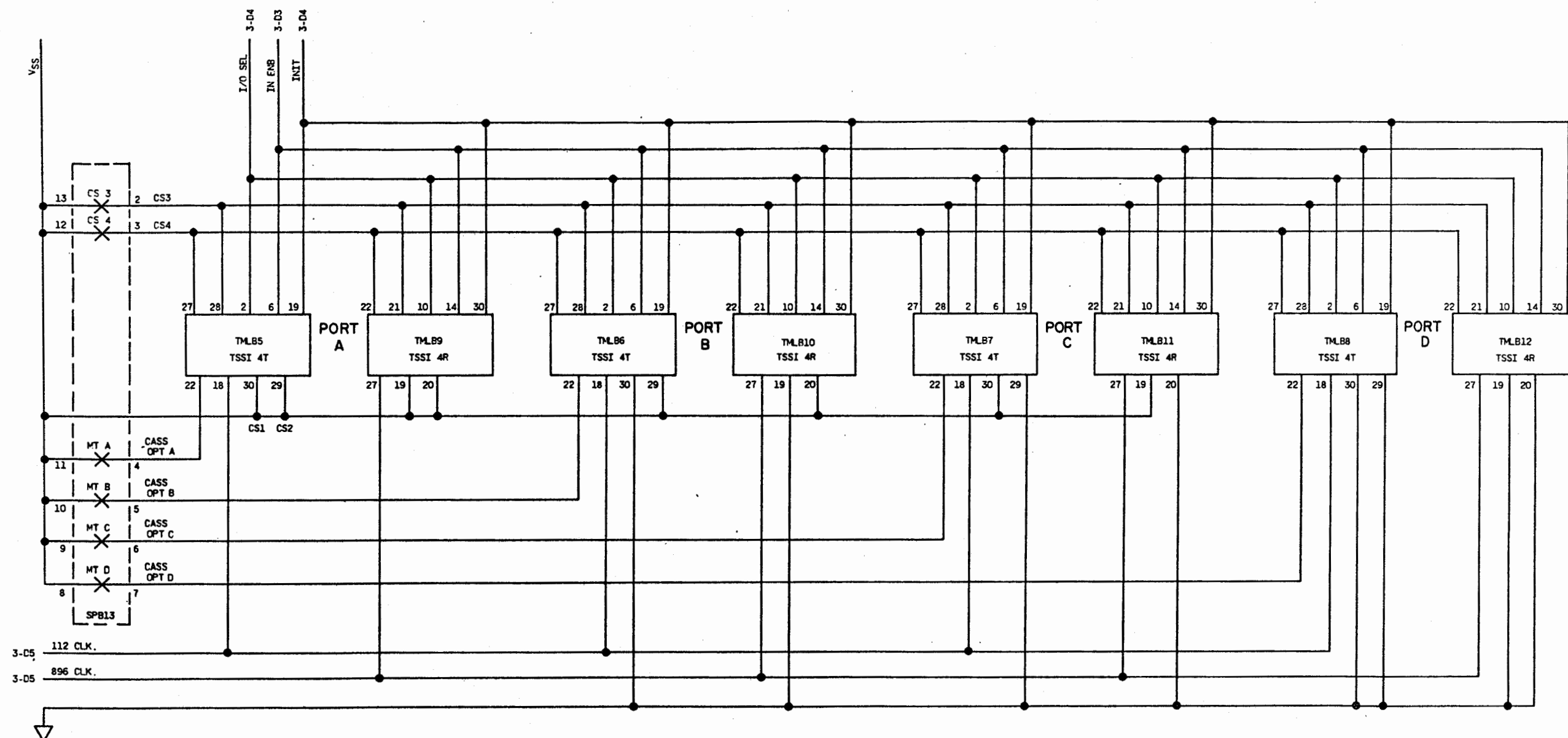
SSI INPUT / OUTPUT
CC406



4406SD-B5

FS-6 CLOCK INPUT AND OPTION LOGIC

ISSUE
1



SSI INPUT / OUTPUT
CC406

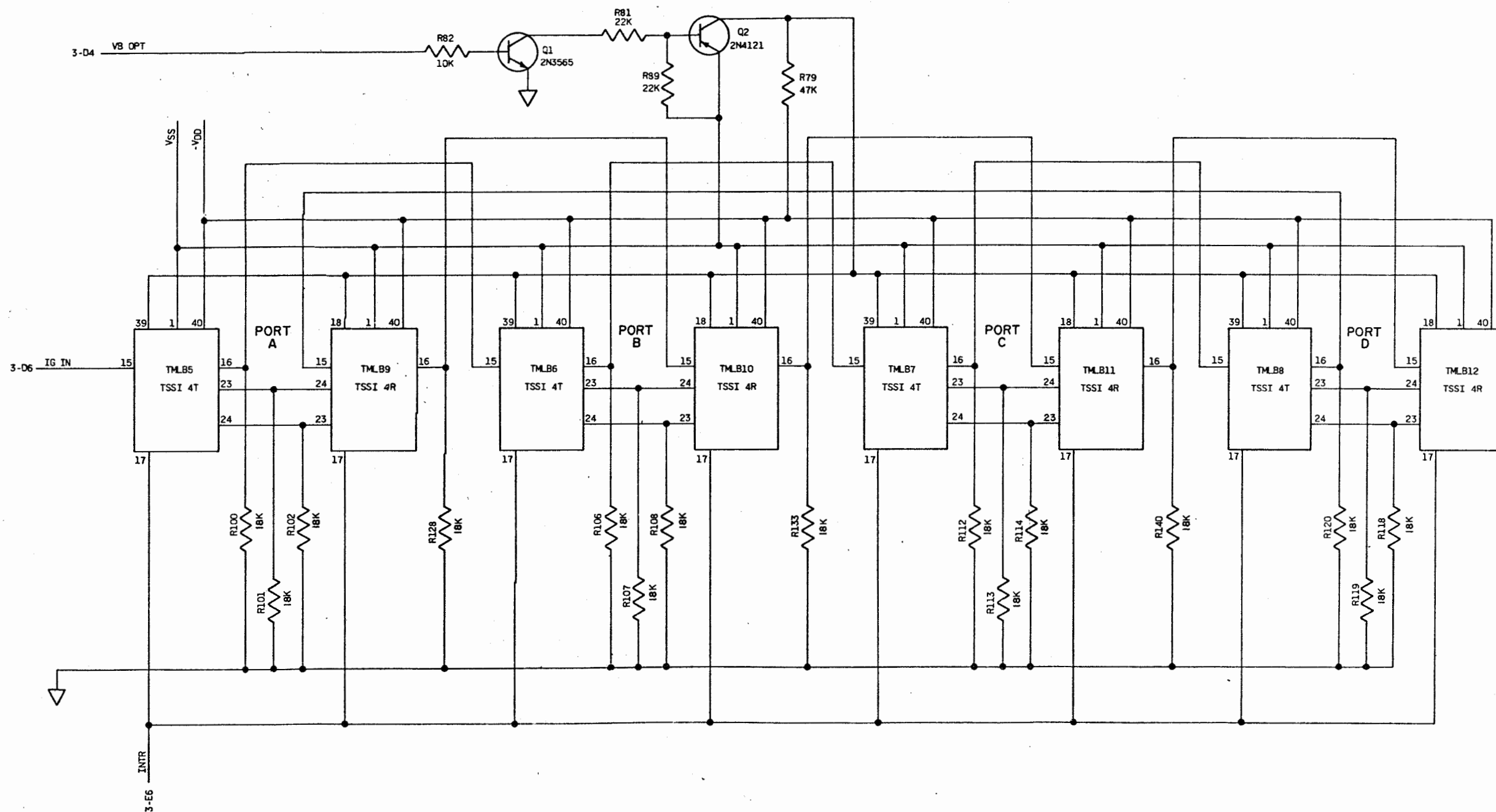


4406SD - B6

NOTE: 1. ON CUSTOMER I.D. ISSUE 6C AND LOWER, THE
VALUE OF R100-R102, R106-R108, R112-R114,
R118-R120, R128, R133 AND R140 IS 6.2K.

FS-7

INTERRUPT LOGIC INTERFACE AND VECTOR OPTION



SSI INPUT/OUTPUT
CC406



4406SD-B7

1

2

3

4

5

6

7

SHEET INDEX

CONTENTS	SHEET NO.	ISSUE NO.																									SHEET NO.
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
SHEET INDEX AND SUPPORTING INFORMATION	1	1																									1
NOTES	2	1																									2
FS1 - TELEBUS INTERFACE	3	1																									3
FS2 - CLOCK CIRCUIT; FS3 - INTERRUPT ARBITRATION	4	1																									4
FS4 - COMMUNICATION INTERFACE UNIT TRANSMITTER	5	1																									5
FS5 - COMMUNICATION INTERFACE UNIT RECEIVER	6	1																									6
FS6 - DIALER INTERFACE UNIT	7	1																									7
FS7 - PROGRAMMABLE INTERVAL TIMER /STATION ID	8	1																									8
FS8 - STATION ID (BITS 0-3)	9	1																									9
FS8 - STATION ID (BITS 4-7)	10	1																									10
FS9 - POWER DISTRIBUTION	11	1																									11
TC1 - TELEBUS SIGNALLING	12	1																									12
TC2 - TYPICAL ASYNCHRONOUS DATA PATTERN	13	1																									13
TC3 - TYPICAL SYNCHRONOUS DATA PATTERN	14	1																									14

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT DESCRIPTION	4411CD

USE OF SHEET INDEX

WHEN CHANGES ARE MADE IN THIS DRAWING:

- ONLY CHANGED SHEETS WILL BE REISSUED, INCLUDING SHEET 1.
- UNCHANGED SHEETS RETAIN EXISTING ISSUE NUMBER.

THE LAST COMPLETED COLUMN ON THE SHEET INDEX INDICATES THE LATEST ISSUE PER SHEET.

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-3-76	24591R

COMMUNICATION INTERFACE UNIT
PIT/SID
CIRCUIT CARD
410411 (CC411)

APPROVALS

PROJ. SUPV. <i>[Signature]</i>	PROJ. DIR. <i>[Signature]</i>	MFG. REL. COMPL. <i>[Signature]</i>
ENGR. DAB	DSGMR.	
DRN.	DATE 2-19-76	
R&D FILE 6-167.1724A		
S-NUMBER		

TELETYPE

4411SD-1

78

Tc 654 (8-71)

CIRCUIT NOTES:

101. VOLTAGE	VOLTAGE RANGE
+12	+10.8 TO +13.2
+5	+4.5 TO +5.5
-12	-10.8 TO -13.2

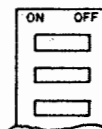
102. INTEGRATED CIRCUIT BATTERY CONNECTIONS:

TYPE	PART NUMBER	+12V	+5V	GRD	-6.2V	-12V
DTL	335528	14		7		1
DTL	335529		14	7		
TTL	339002		14	7		
TTL	339138		16	8		
TTL	339161		16	8		
TTL	339347		16	8		
TTL	339404		14	7		
TTL	339438		14	7		
TTL	339837		16	8		
TTL	339838		16	8		
MOS	342290		1		40	20
MOS	342291		1		40	20
MOS	342292		1		40	20
TTL	339251		16	8		

103. SWITCH PROGRAMMING:

CLOSE SWITCH (ON) TO PROGRAM
A LOGICAL '0'.

OPEN SWITCH (OFF) TO PROGRAM
A LOGICAL '1'.



DEPRESS ON OR DOT SIDE
OF SWITCH TO CLOSE.
SWITCH 1 (SW1) IS ALWAYS
ORIENTED TOWARD THE TOP
OF THE CIRCUIT CARD.

ASYNCHRONOUS BAUD RATE SELECTION

BAUD RATE	SPA21							
	SW2	SW3	SW4	SW5	SW6	SW7	SW8	
	SPEED 2 BAUD RATE TABLE BIT 7=0 IN CONTROL REGISTER 1				SPEED 1 BAUD RATE TABLE BIT 7=1 IN CONTROL REGISTER 1			
50	OFF	OFF	OFF	ON	OFF	OFF	OFF	
75	OFF	OFF	ON	ON	ON	OFF	OFF	
100	OFF	ON	OFF	ON	OFF	ON	OFF	
110	OFF	ON	ON	ON	ON	ON	OFF	
150	ON	OFF	OFF	ON	OFF	OFF	ON	
300	ON	OFF	ON	ON	ON	OFF	ON	
450	ON	ON	OFF	ON	OFF	ON	ON	
600	ON	ON	ON	ON	ON	ON	ON	
300	OFF	OFF	OFF	OFF				
450	OFF	OFF	ON	OFF				
600	OFF	ON	OFF	OFF				
900	OFF	ON	ON	OFF				
1200	ON	OFF	OFF	OFF				
1800	ON	OFF	ON	OFF				
2400	ON	ON	OFF	OFF				
3600	ON	ON	ON	OFF				

SYNC / ISOC LOOPBACK TEST BAUD RATE SELECTION

BAUD RATE	SPA21			
	SW2	SW3	SW4	SW5
800	OFF	OFF	OFF	ON
1200	OFF	OFF	ON	ON
1600	OFF	ON	OFF	ON
1760	OFF	ON	ON	ON
2400	ON	OFF	OFF	ON
4800	ON	OFF	ON	ON
7200	ON	ON	OFF	ON
9600	ON	ON	ON	ON
4800	OFF	OFF	OFF	OFF
7200	OFF	OFF	ON	OFF
9600	OFF	ON	OFF	OFF
14400	OFF	ON	ON	OFF
19200	ON	OFF	OFF	OFF
28800	ON	OFF	ON	OFF
38400	ON	ON	OFF	OFF
57600	ON	ON	ON	OFF

103. (CONTINUED)

DESIGNATION	FUNCTION	SWITCH STATE (TO ENABLE FUNCTION)
SPA21 - SW9	"MODEM CHECK" FROM MODEM STRAPPED PERMANENTLY "OFF"	OFF
SPB12	SW1 BIT 7	ON = LOGIC '0' ON T.1 EBUS
	SW2 BIT 6	
	SW3 BIT 5	
	SW4 BIT 4	
SPB12	SW5 BIT 5	ON = LOGIC '0' ON TELEBUS
	SW6 BIT 6	
	SW7 BIT 7	
	SW8	
	FACTORY TEST SWITCH: WHEN SWITCH IS OPEN, LOCAL CLOCK ON CARD IS ISOLATED FROM LOGIC FOR FACTORY TEST PURPOSES.	ON (THIS SWITCH MUST BE CLOSED FOR PROPER CARD OPERATION)
SPA21-SW1	"CARRIER DETECT" FROM MODEM STRAPPED PERMANENTLY "ON"	ON

SID SWITCH PROGRAMMING INFORMATION

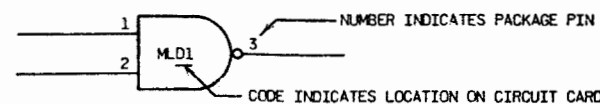
	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
WORD 0	SPB1 SW1	SPB2 SW1	SPB3 SW1	SPB4 SW1	SPB5 SW1	SPB6 SW1	SPB7 SW1	SPB8 SW1
WORD 1	SPB1 SW2	SPB2 SW2	SPB3 SW2	SPB4 SW2	SPB5 SW2	SPB6 SW2	SPB7 SW2	SPB8 SW2
WORD 2	SPB1 SW3	SPB2 SW3	SPB3 SW3	SPB4 SW3	SPB5 SW3	SPB6 SW3	SPB7 SW3	SPB8 SW3
WORD 3	SPB1 SW4	SPB2 SW4	SPB3 SW4	SPB4 SW4	SPB5 SW4	SPB6 SW4	SPB7 SW4	SPB8 SW4
WORD 4	SPB1 SW5	SPB2 SW5	SPB3 SW5	SPB4 SW5	SPB5 SW5	SPB6 SW5	SPB7 SW5	SPB8 SW5
WORD 5	SPB1 SW6	SPB2 SW6	SPB3 SW6	SPB4 SW6	SPB5 SW6	SPB6 SW6	SPB7 SW6	SPB8 SW6
WORD 6	SPB1 SW7	SPB2 SW7	SPB3 SW7	SPB4 SW7	SPB5 SW7	SPB6 SW7	SPB7 SW7	SPB8 SW7
WORD 7	SPB1 SW8	SPB2 SW8	SPB3 SW8	SPB4 SW8	SPB5 SW8	SPB6 SW8	SPB7 SW8	SPB8 SW8

INFORMATION NOTES:

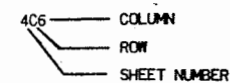
201. ALL RESISTORS 1/4 WATT AND RESISTANCE VALUE IN OHMS, UNLESS SPECIFIED.
202. ALL CAPACITOR VALUES IN MICROFARADS, UNLESS SPECIFIED.

203. → INDICATES MALE TERMINAL.

204. LOGIC DESIGNATION

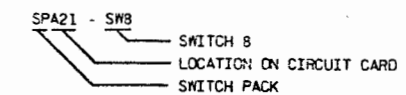


205. CROSS REFERENCE DESIGNATOR

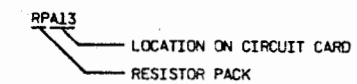


INFORMATION NOTES: (CONTINUED)

206. SWITCH PACK DESIGNATION



207. RESISTOR PACK DESIGNATION



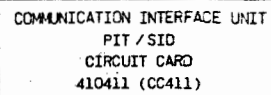
208. POSITIVE LOGIC SYMBOLS ARE EMPLOYED

COMMUNICATION INTERFACE UNIT
PIT / SID
CIRCUIT CARD
410411 (CC411)



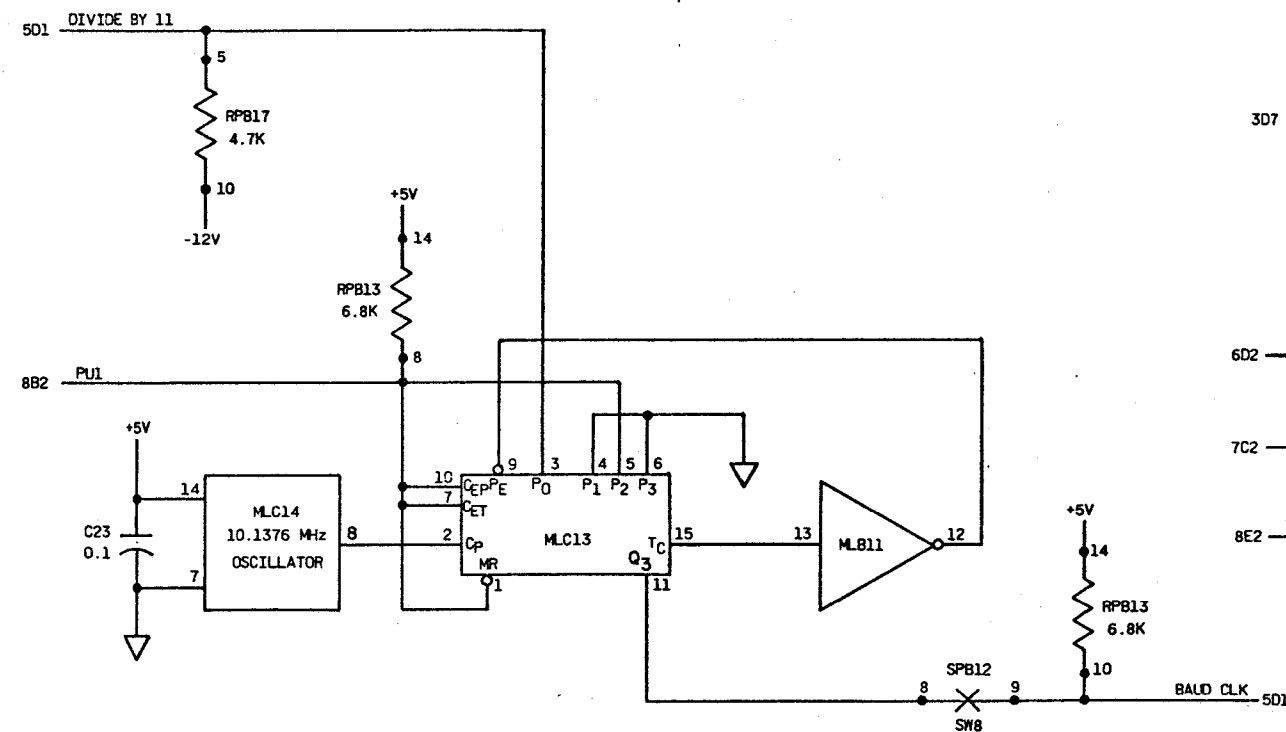
4411SD-2

ISSUE
1

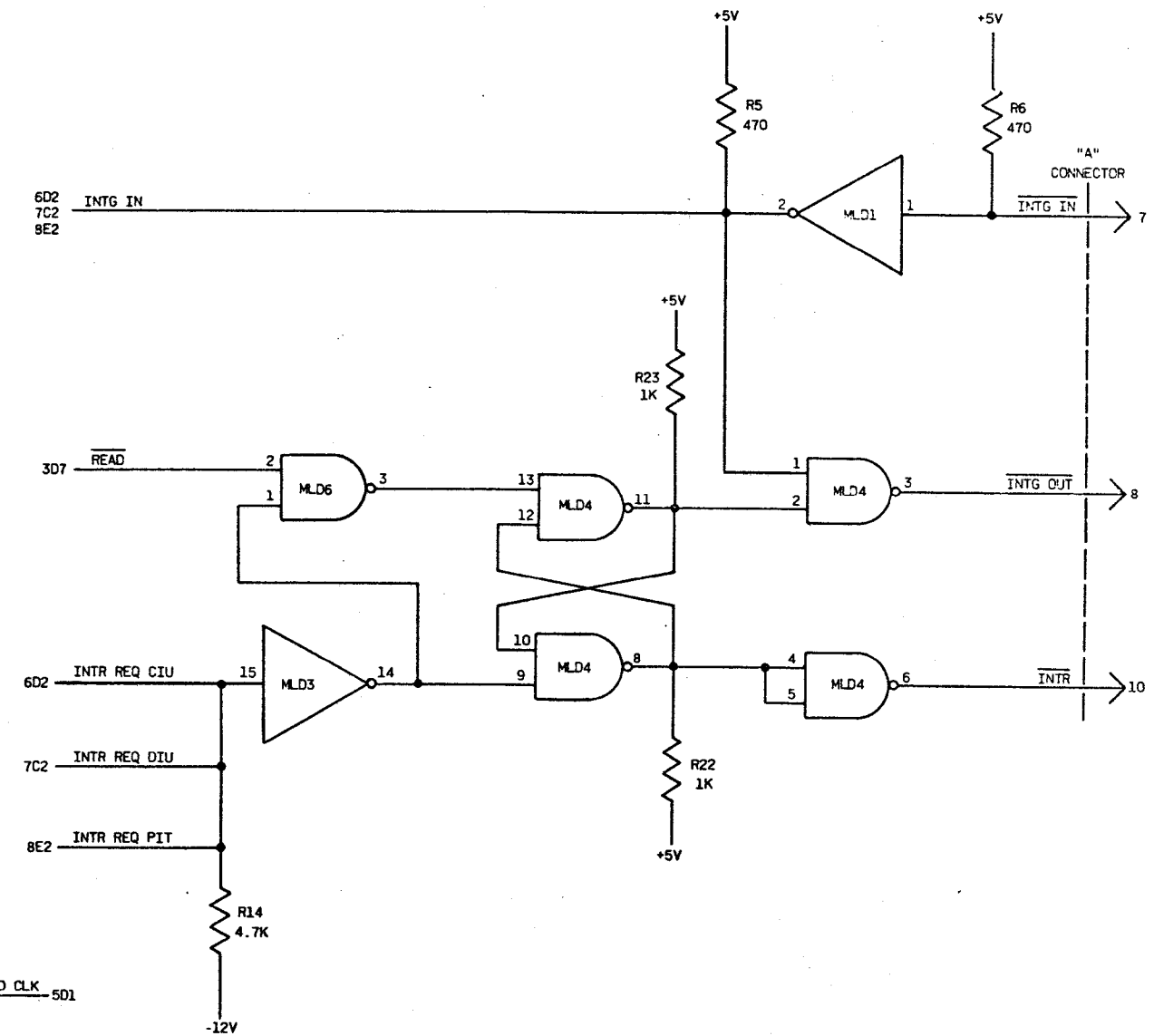


4411SD-3

FS2-CLOCK CIRCUIT



FS3-INTERRUPT ARBITRATION



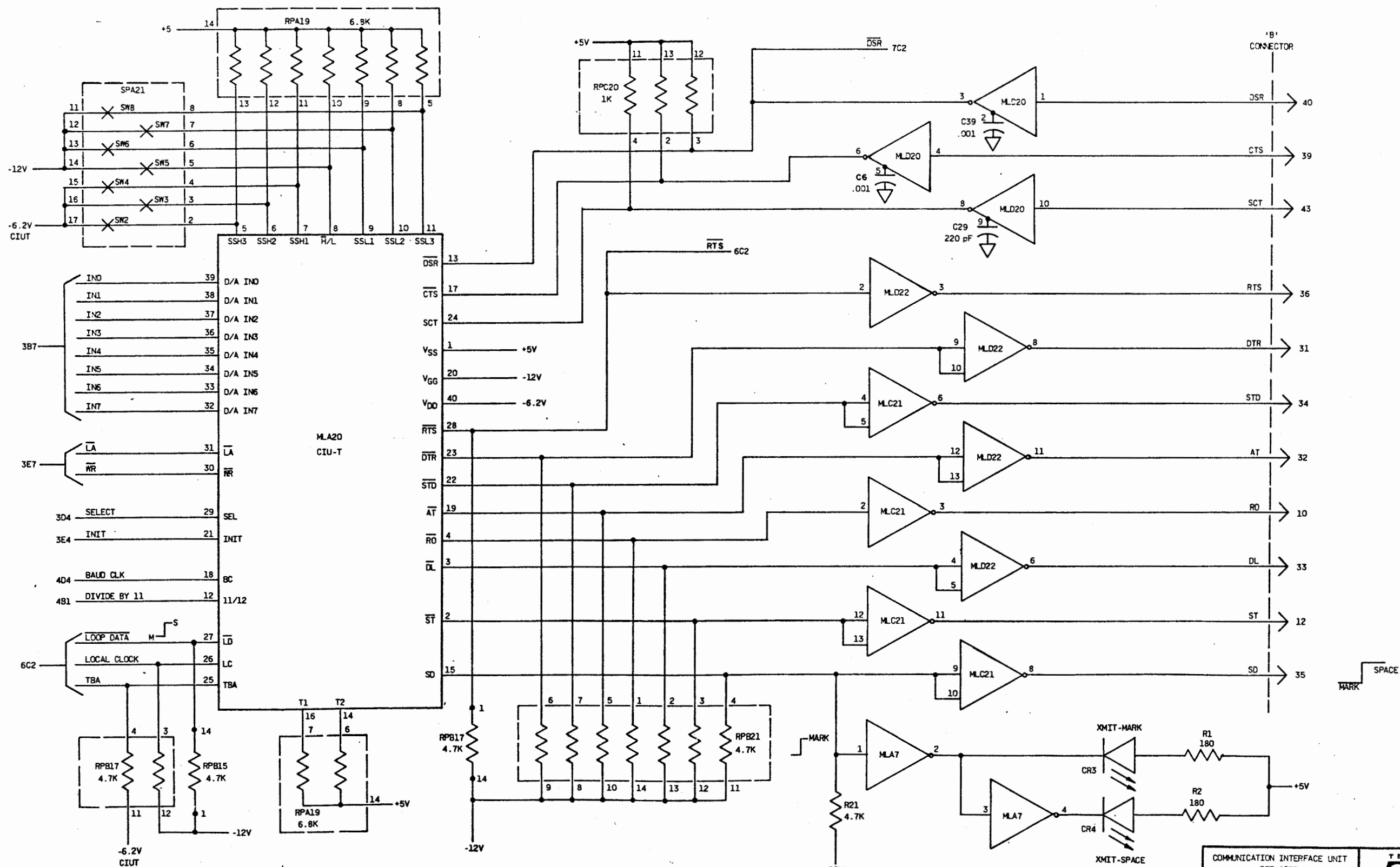
COMMUNICATION INTERFACE UNIT
PIT / SID
CIRCUIT CARD
410411 (CC411)



4411SD-4

FS4-COMMUNICATION INTERFACE UNIT TRANSMITTER

ISSUE
1



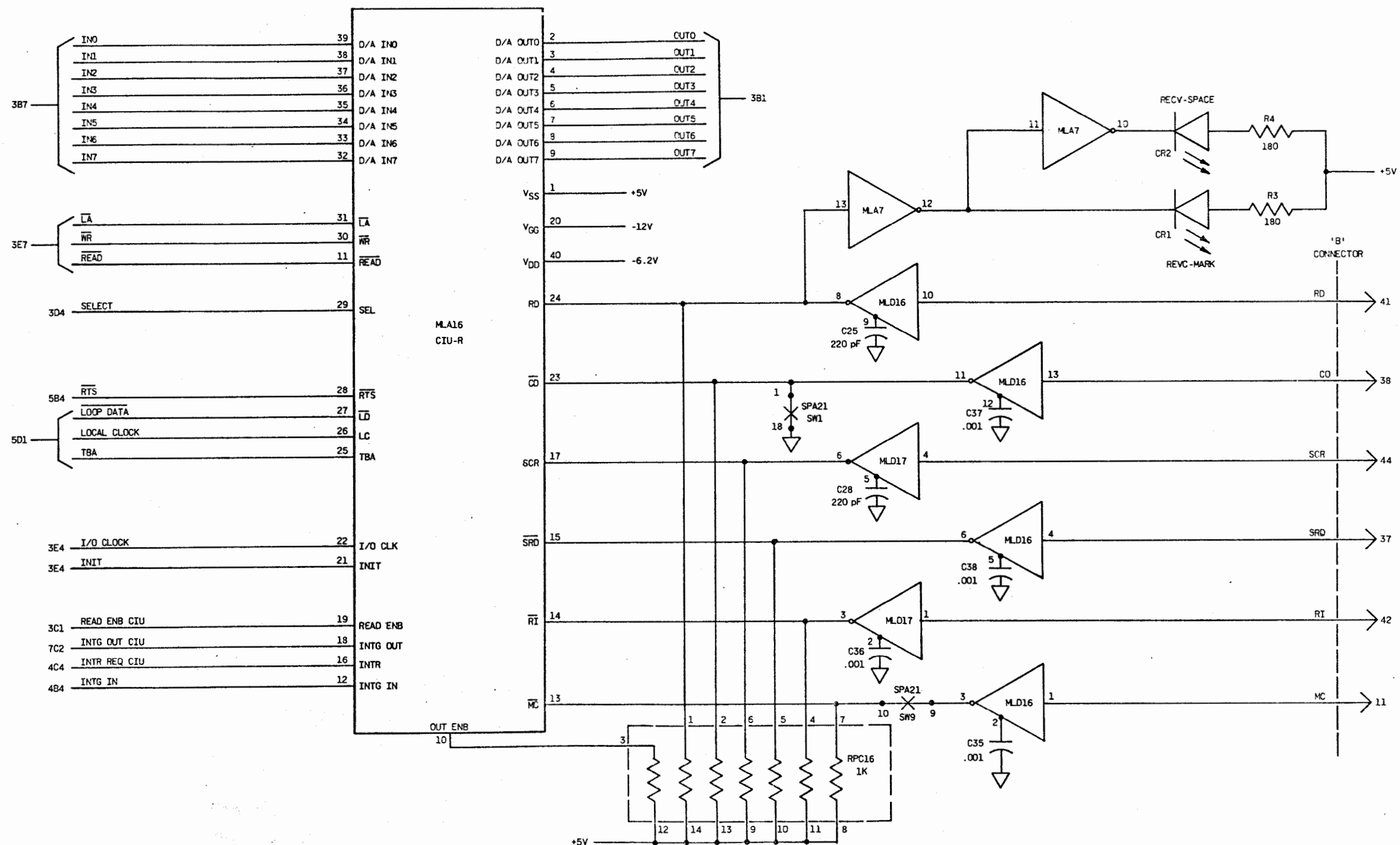
COMMUNICATION INTERFACE UNIT
PIT / SID
CIRCUIT C/ID
410411 (C0411)



4411SD-5

FS5-COMMUNICATION INTERFACE UNIT RECEIVER

ISSUE
1

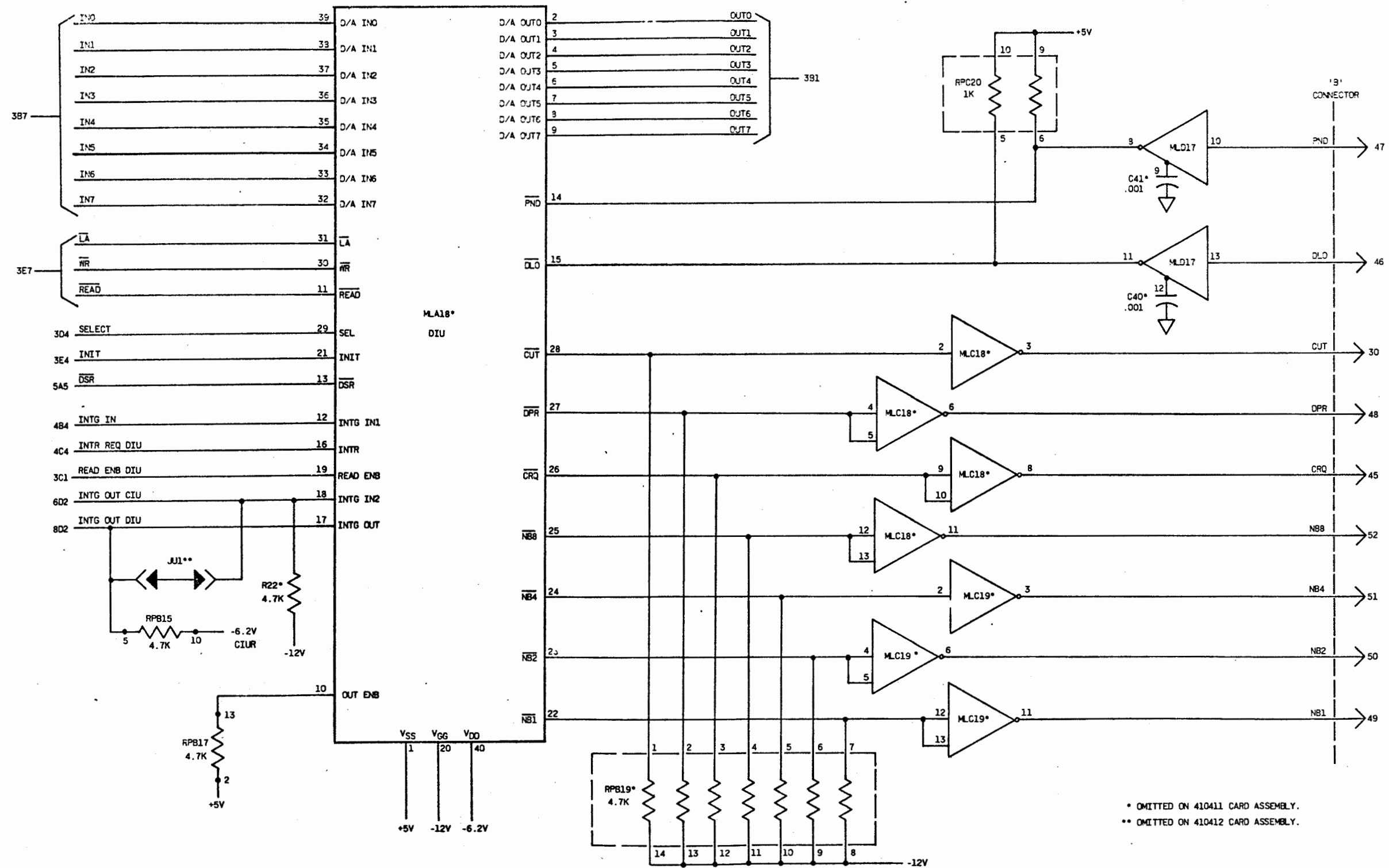


COMMUNICATION INTERFACE UNIT
PIT / SID
CIRCUIT CARD
410411 (CC411)



4411SD-6

FS6-DIALER INTERFACE UNIT



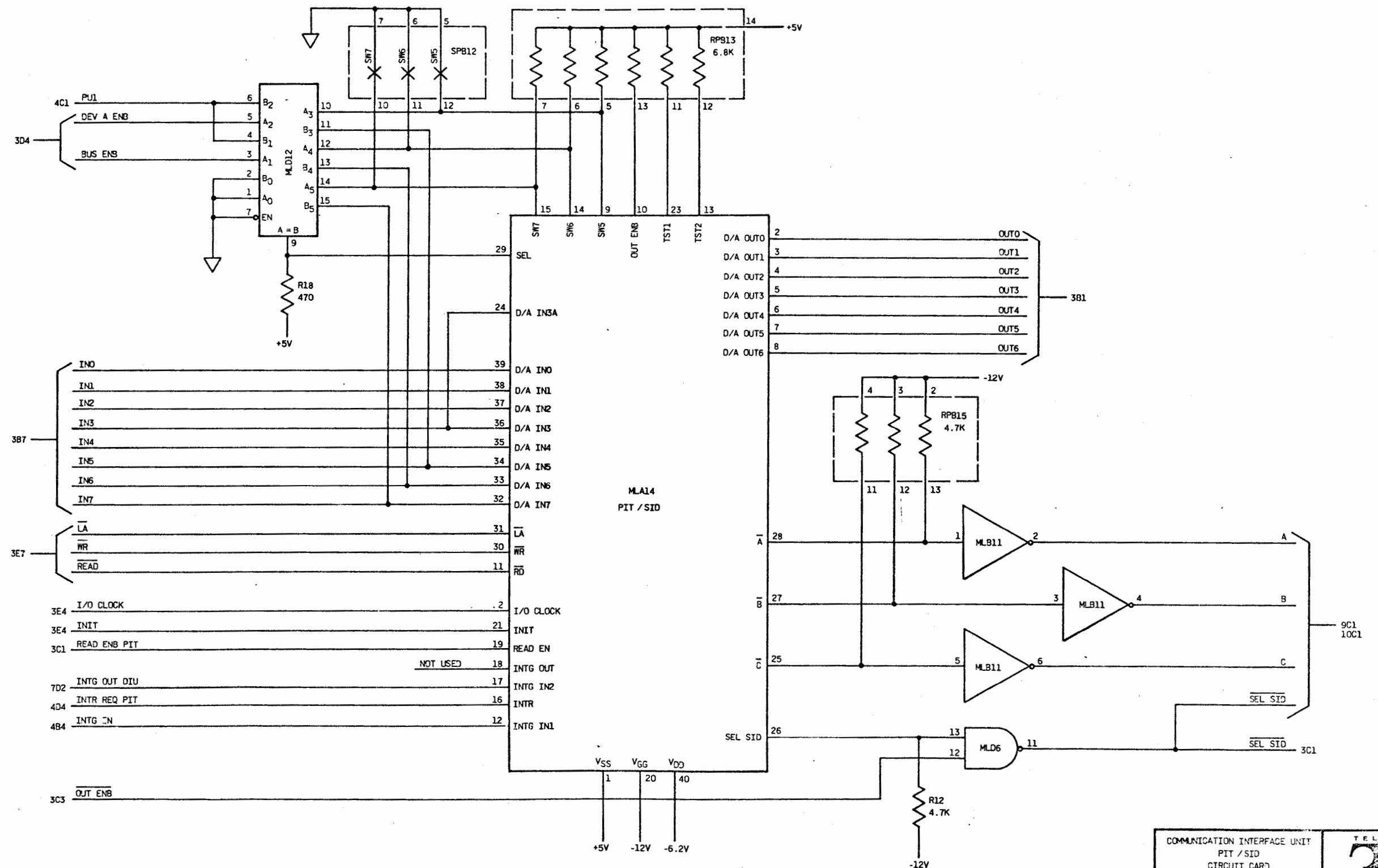
* OMITTED ON 410411 CARD ASSEMBLY.
 ** OMITTED ON 410412 CARD ASSEMBLY.

COMMUNICATION INTERFACE UNIT
 PIT / SID
 CIRCUIT CARD
 410411 (CC411)



4411SD-7

FS7-PROGRAMMABLE INTERVAL TIMER/STATION ID



COMMUNICATION INTERFACE UNIT
PIT / SID
CIRCUIT CARD
410411 (CC411)



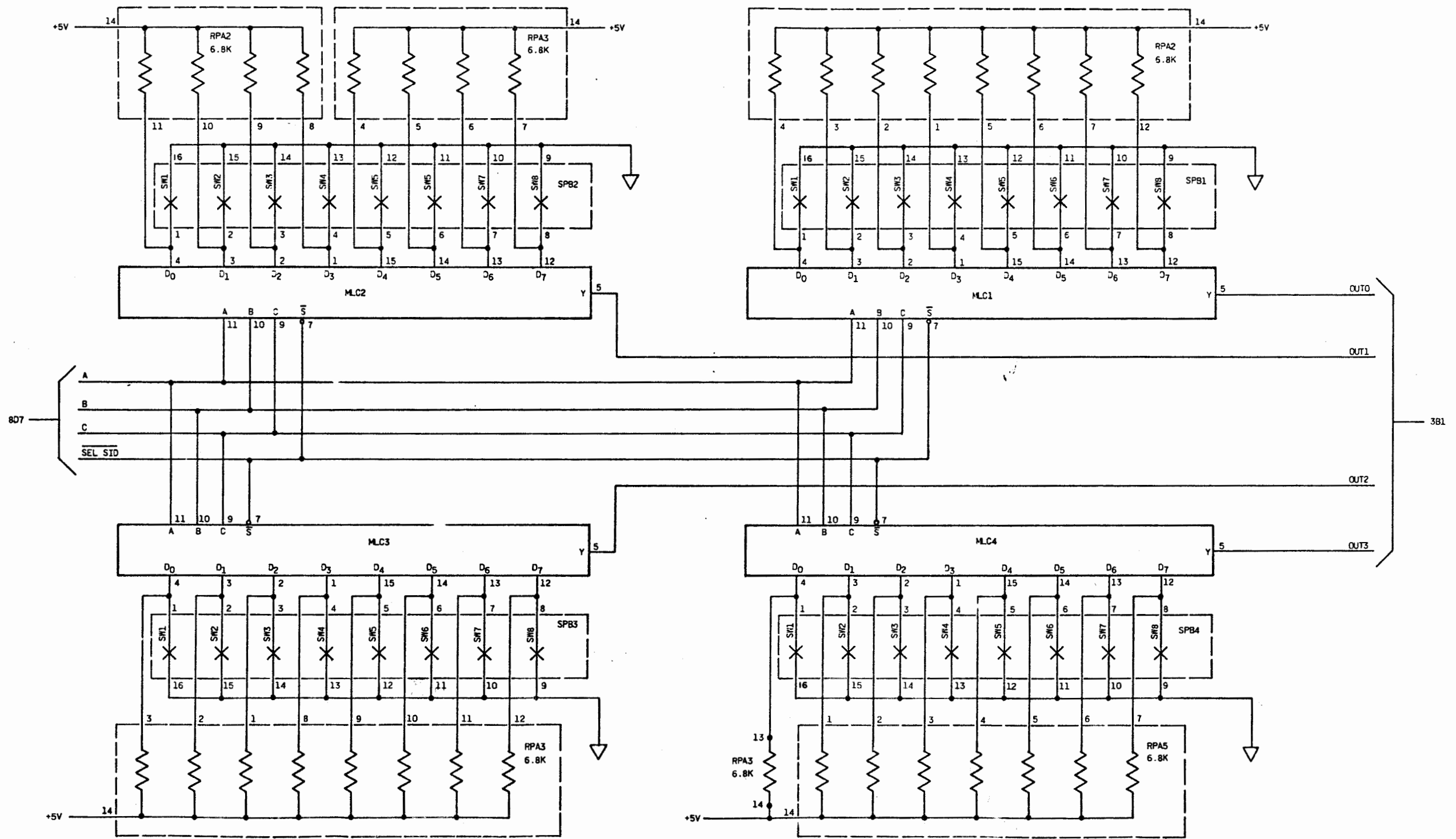
44IISD-8

85

FS8-STATION ID (BITS 0-3)

ISSUE
1

A
B
C
D
E



COMMUNICATION INTERFACE UNIT
PIT / SID
CIRCUIT CARD
410411 (CC411)

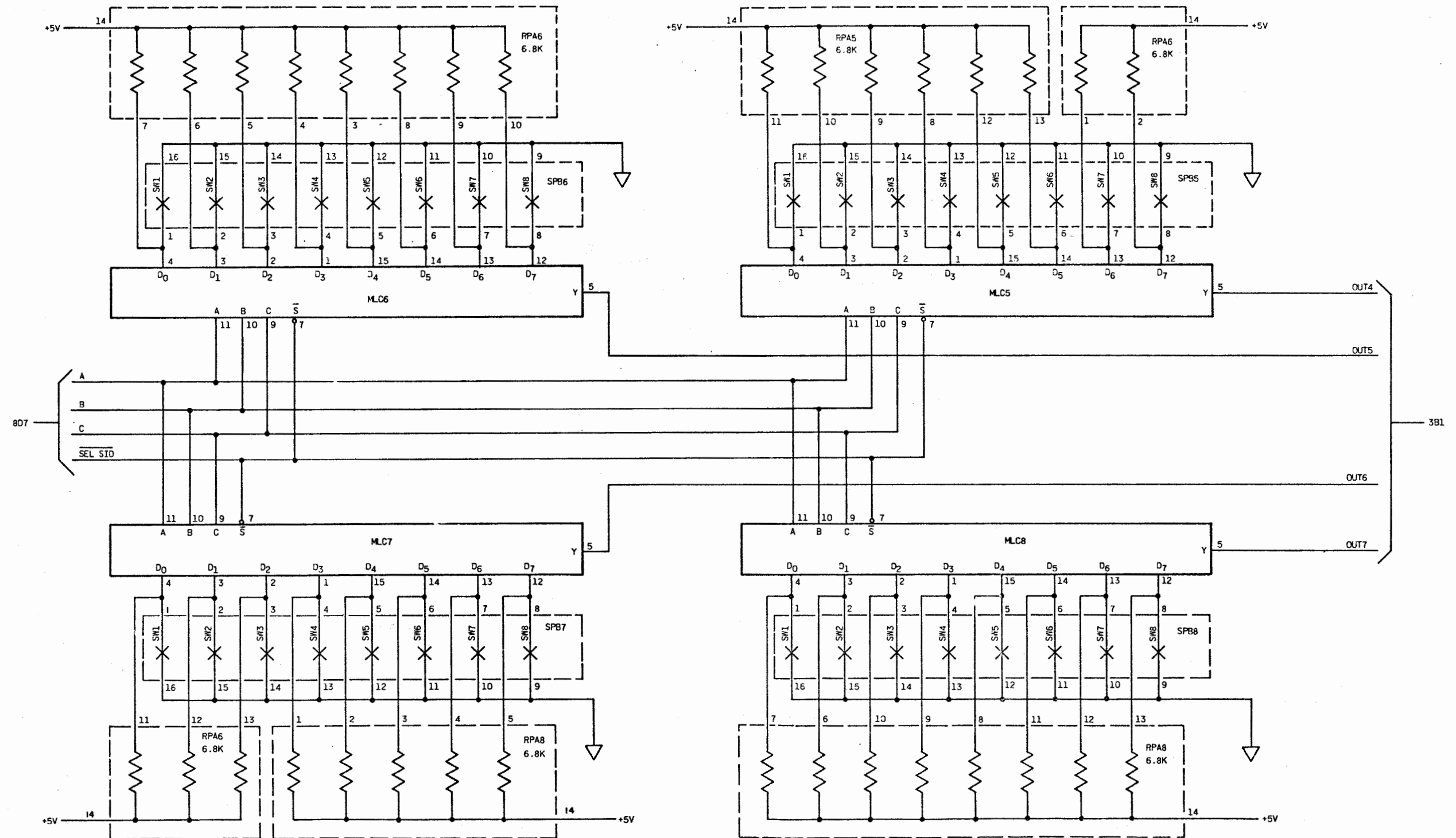


4411SD-9

86

FS8-STATION ID (BITS 4-7)

ISSUE
1



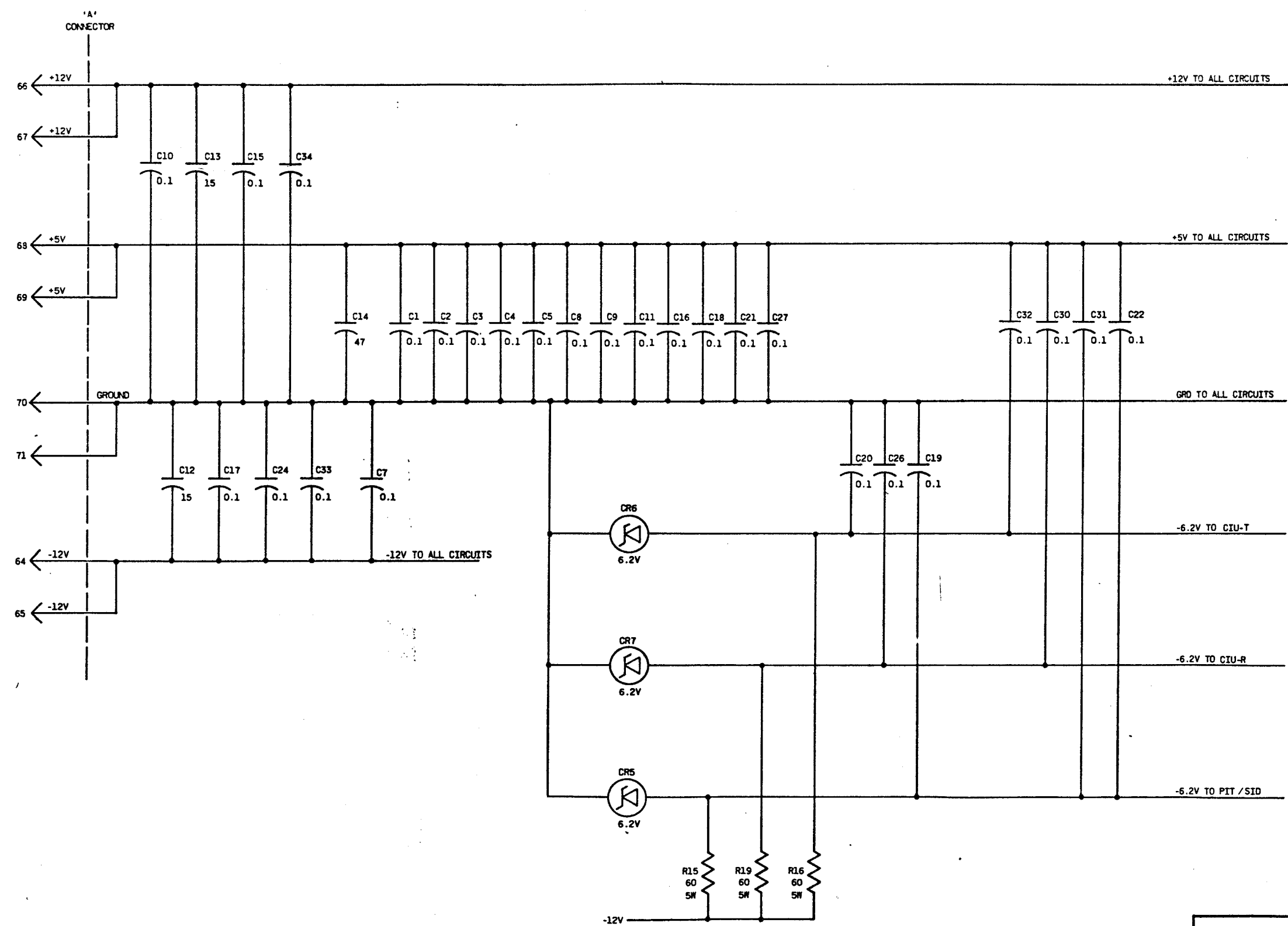
COMMUNICATION INTERFACE UNIT
PIT / SID
CIRCUIT CARD
410411 (C0411)



4411SD-10

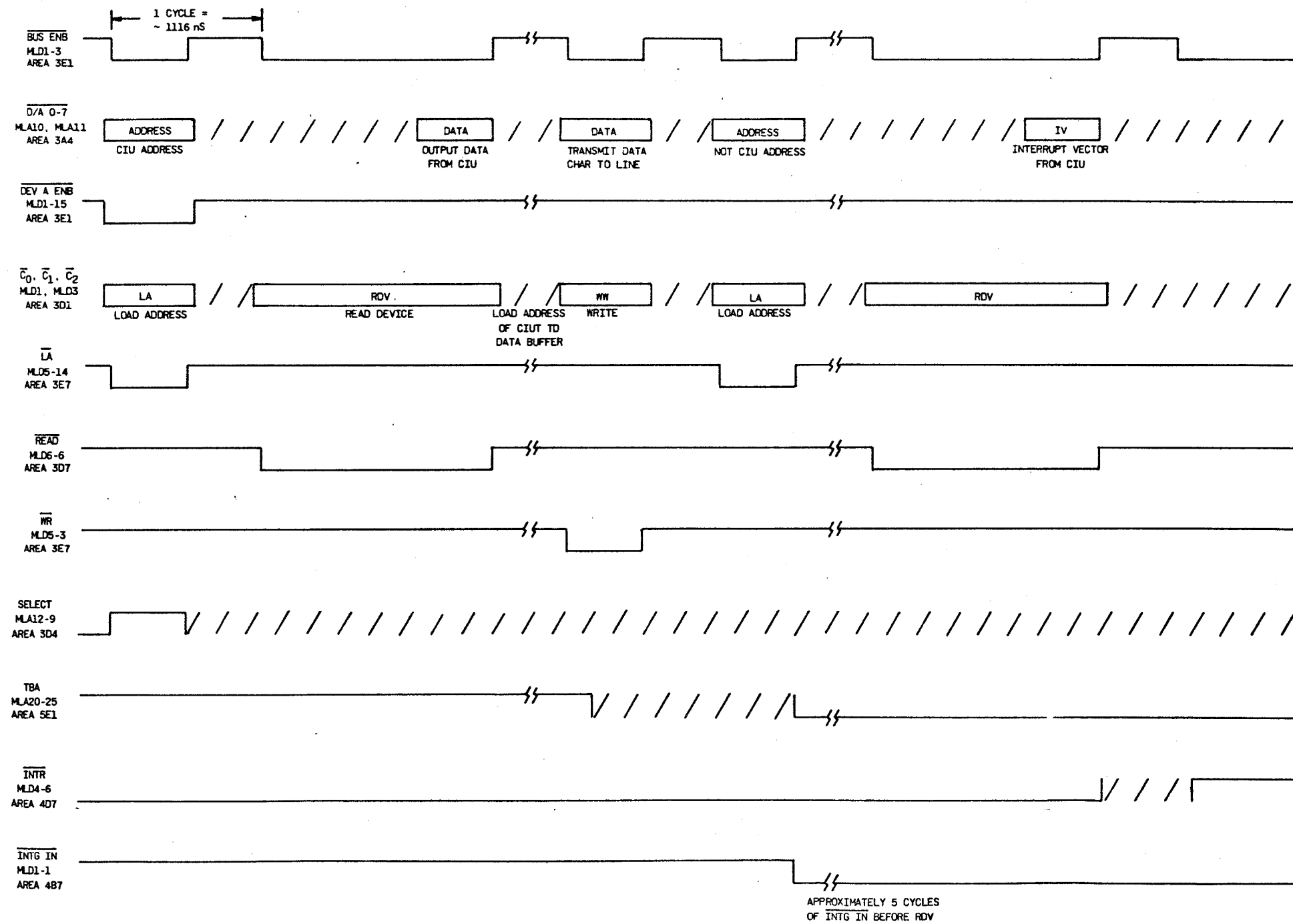
FS9-POWER DISTRIBUTION

ISSUE
1



COMMUNICATION INTERFACE UNIT PIT / SID CIRCUIT CARD 410411 (CC411)	TELETYPE
	44IISD-II

TC1 TELEBUS SIGNALLING



COMMUNICATION INTERFACE UNIT
PIT / SID
CIRCUIT CARE
410411 (CC411)



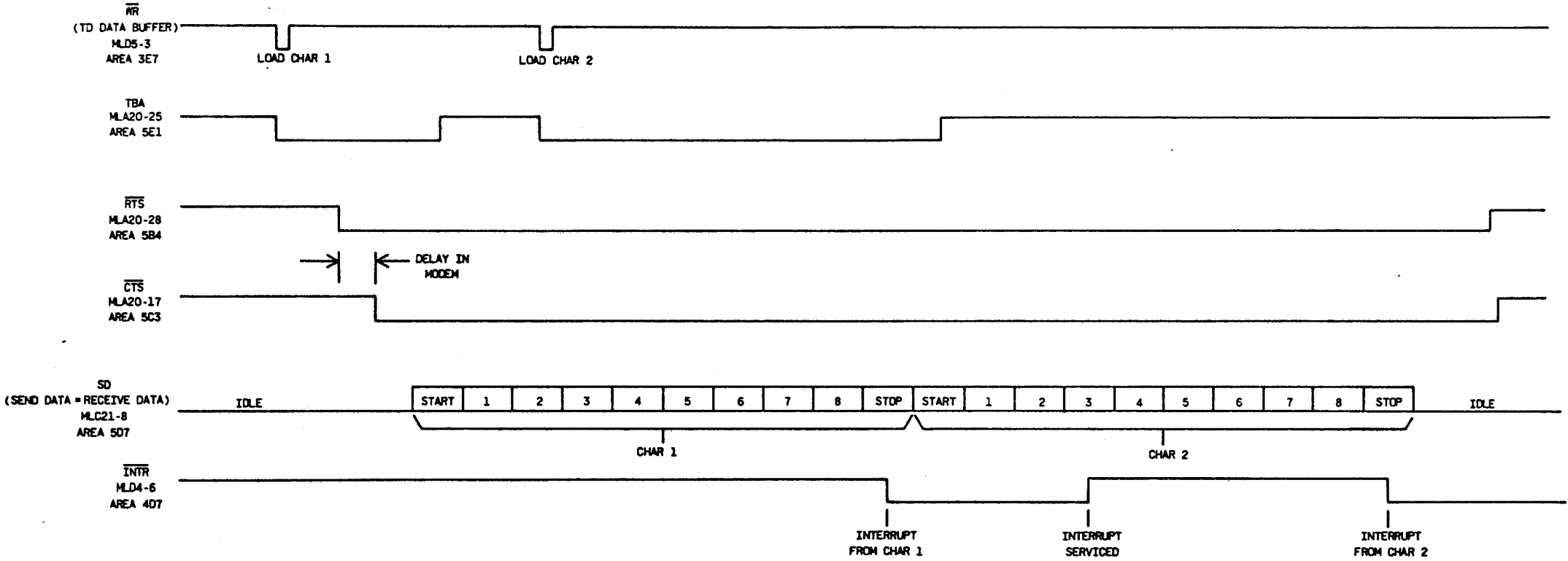
4411SD-12

ISSUE
1

A
B
C
D
E

TC2 TYPICAL ASYNCHRONOUS DATA PATTERN

MODE: ANALOG LOOP, INTERRUPT ENABLE ON, 10 BIT OPERATION



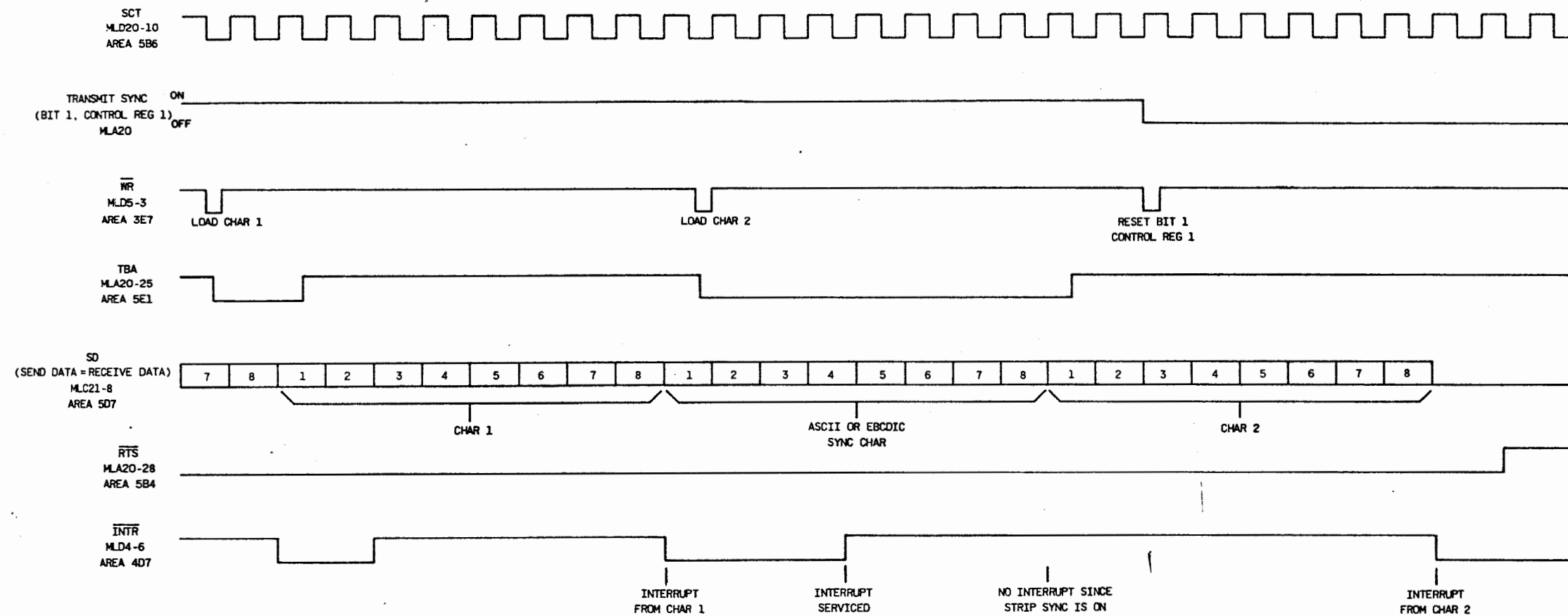
COMMUNICATION INTERFACE UNIT
PIT / SID
CIRCUIT CARD
410411 (CC411)



4411SD-13

TC3 TYPICAL SYNCHRONOUS DATA PATTERN

MODE: ANALOG LOOP, INTERRUPT ENABLE ON, STRIP SYNC ON



COMMUNICATION INTERFACE UNIT
PIT / SID
CIRCUIT CARD
410411 (CC411)



4411SD-14

ISSUE
1

A
B
C
D
E

SHEET INDEX

CONTENTS	SHEET NO.	ISSUE NO.																									SHEET NO.
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
SHEET INDEX, SUPPORTING INFORMATION, AND BLOCK DIAGRAM	1	1	2	3	4	5																					1
BUS INTERFACE AND INPUT CACHE	2	1	1	1	1	3																					2
DISPLAY CACHE, FONT ROMS, AND ATTRIBUTE LOGIC	3	1	2	2	2	4																					3
VIDEO LOGIC	4	1	1	1	2	3																					4
TIMING AND CONTROL LOGIC	5	1	2	3	4	5																					5

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT DESCRIPTION	44300D

USE OF SHEET INDEX

WHEN CHANGES ARE MADE IN THIS DRAWING:

- ONLY CHANGED SHEETS WILL BE REISSUED. (INCLUDING SHEET 1)
- UNCHANGED SHEETS RETAIN EXISTING ISSUE NUMBER.

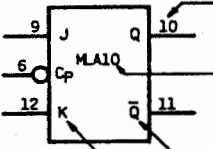
THE LAST COMPLETED COLUMN ON THE SHEET INDEX INDICATES THE LATEST ISSUE PER SHEET.

REVISIONS

ISSUE	DATE	AUTH. NO.
1	2-6-75	23774-R
2	5-14-75	14156
3	8-5-76	16250
4	8-31-76	16509
5	10-10-77	18818

NOTES:

- UNLESS OTHERWISE INDICATED, +5V IS APPLIED TO PIN 14 OF 14 PIN PACKAGES AND PIN 16 OF 16 PIN PACKAGES. GROUND IS APPLIED TO PIN 7 OF 14 PIN PACKAGES AND PIN 8 OF 16 PIN PACKAGES.

- 

NUMBERS REFER TO PACKAGE PIN

INDICATES PACK LOCATION ON THE CIRCUIT CARD

INDICATES LOGIC FUNCTION

3. SHEET LOCATION CODE

- 1-A-5
- INDICATES X-Y COORDINATES ON DISTANT SHEET
- INDICATES DISTANT SHEET NUMBER

4. CONNECTOR CODE

- A13
- INDICATES MALE PIN
- INDICATES PIN NUMBER
- INDICATES A OR B CONNECTOR

5. CONNECTOR PIN ASSIGNMENT

CONNECTOR	PIN	DESCRIPTION	SHEET LOCATION
A	3	BUS ENABLE	501
A	7	INTG. IN	501
A	8	INTG. OUT	501
A	10	INTR	501
A	15	INITIALIZE	501
A	19	C0	501
A	21	C1	501
A	23	C2	501
A	25	D/A0	281
A	27	D/A1	2A1
A	29	D/A2	2A1
A	31	D/A3	2A1
A	33	D/A4	281
A	35	D/A5	281
A	37	D/A6	2C1
A	39	D/A7	2C1
A	41	D/A8	281
A	43	D/A9	281
A	45	D/A10	281
A	47	D/A11	281
A	49	D/A12	2C1
A	51	D/A13	2C1
A	53	D/A14	2C1
A	55	D/A15	2C1
A	64	-12V	301
A	65	-12V	301
A	68	+5V	301
A	69	+5V	301
A	70	GND	301
A	71	GND	301

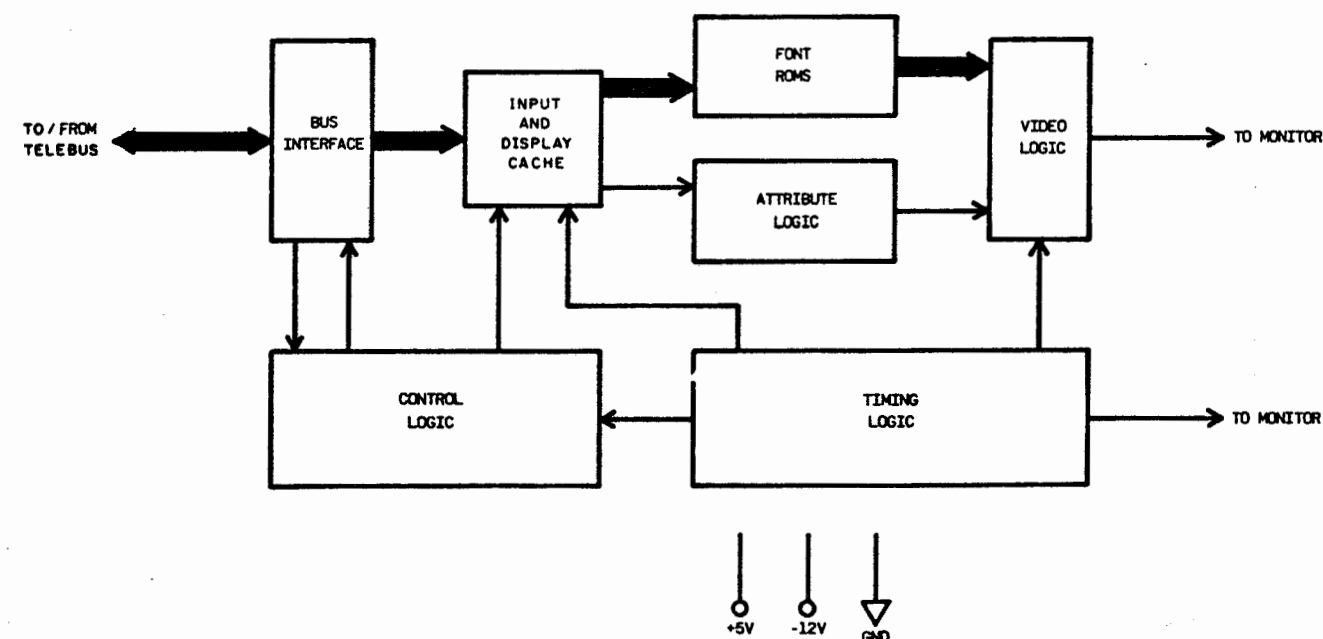
CONNECTOR	PIN	DESCRIPTION	SHEET LOCATION
B	64	HALF INTENSITY	4A7
B	65	HALF INTENSITY	4A7
B	66	VIDEO	4A7
B	67	VIDEO	4A7
B	68	HORIZ. DRIVE	4D7
B	69	HORIZ. RETURN	4D7
B	70	VERT. RETRACE	5E7
B	71	VERT. RETURN	5E7

6. VECTOR SWITCH PROGRAMMING

- 1 "ON" - SWITCH CLOSED
- 2 "OFF" - SWITCH OPEN
- 3 MOVE SWITCH TO "ON" SIDE OR
- 4 PRESS DOT SIDE TO CLOSE.

VECTOR PAIRS	SWITCH NUMBER		
	1	2	3
0 & 2	ON	ON	ON
4 & 6	ON	ON	OFF
10 & 12	ON	OFF	ON
14 & 16	ON	OFF	OFF
400 & 402	OFF	ON	ON
404 & 406	OFF	ON	OFF
410 & 412	OFF	OFF	ON
414 & 416	OFF	OFF	OFF

BLOCK DIAGRAM

SCHEMATIC
DIAGRAM
FOR
DIO CARD

APPROVALS

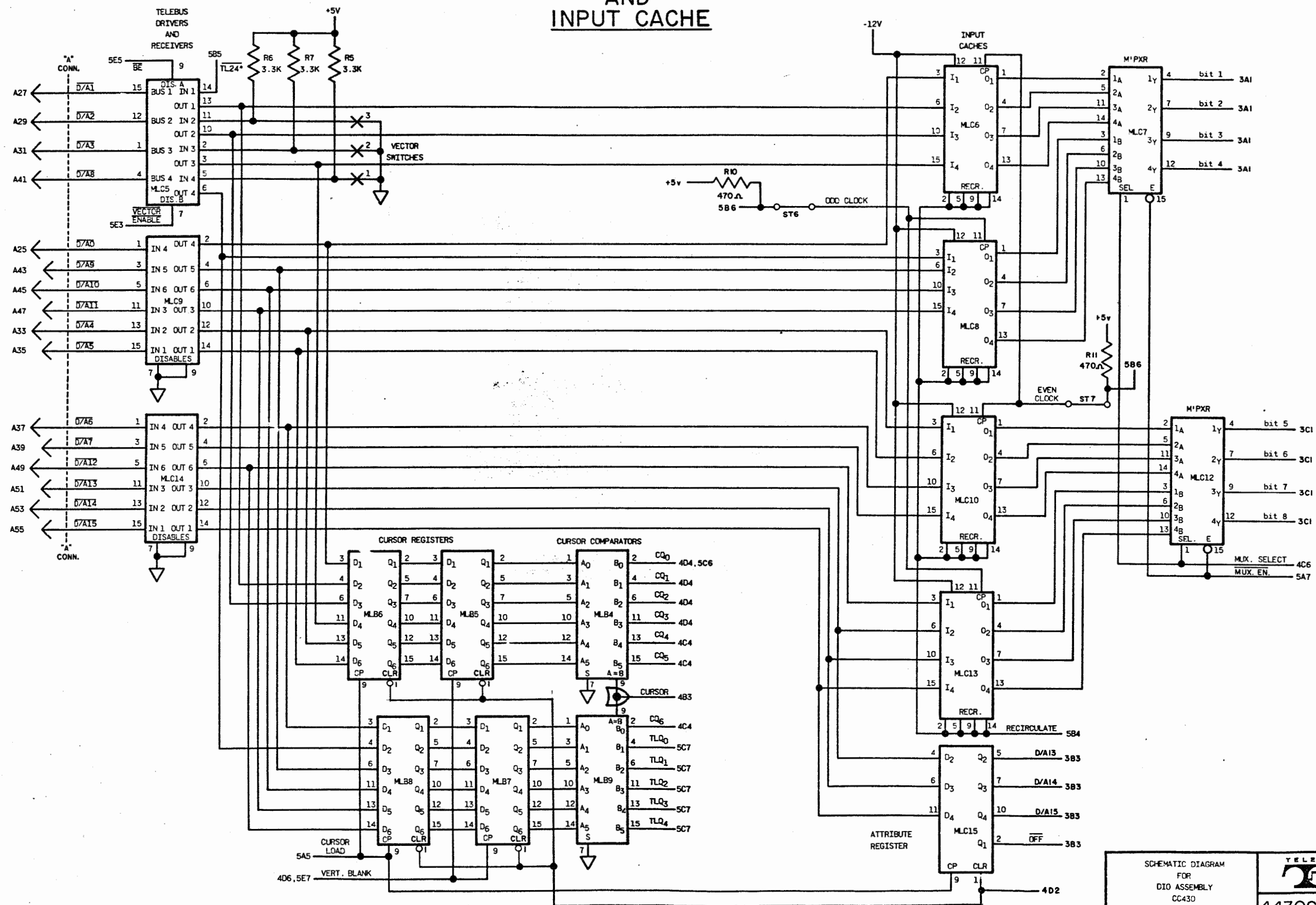
PROJ. SUPV.	PROJ. ENGR.	MFG. REL. COMPL.
ENGR. JMG	OSGMR.	
DRN. TRUHN	DATE	
R & D FILE	2-176.172AA	
S-NUMBER		

TELETYPE
T

4430SD-1

BUS INTERFACE AND INPUT CACHE

ISSUE
1
2
3

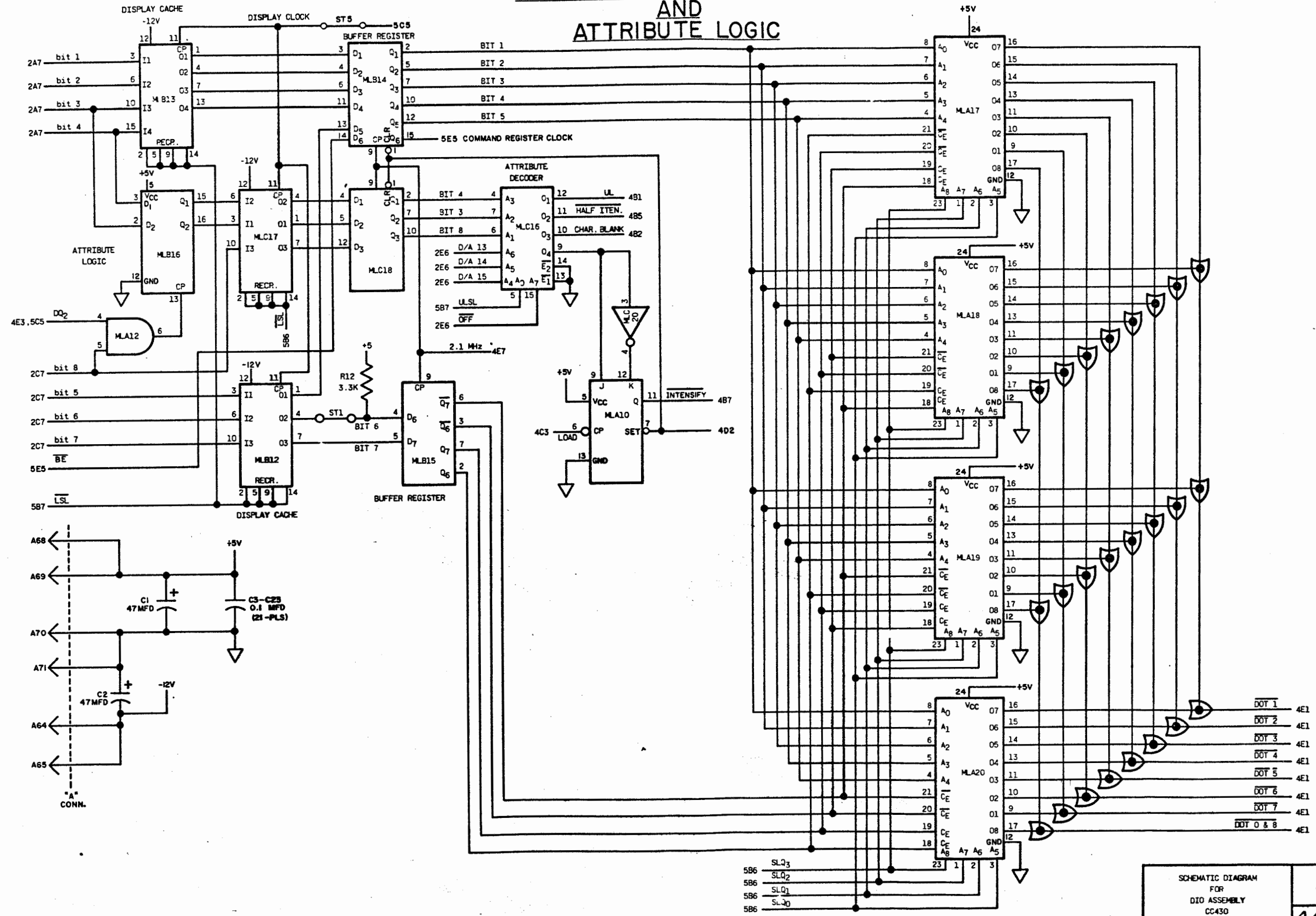


SCHEMATIC DIAGRAM
FOR
DIO ASSEMBLY
CC430

TELETYPE
4430SD-2

DISPLAY CACHE, FONT ROMS AND ATTRIBUTE LOGIC

ISSUE
1
2
3
4



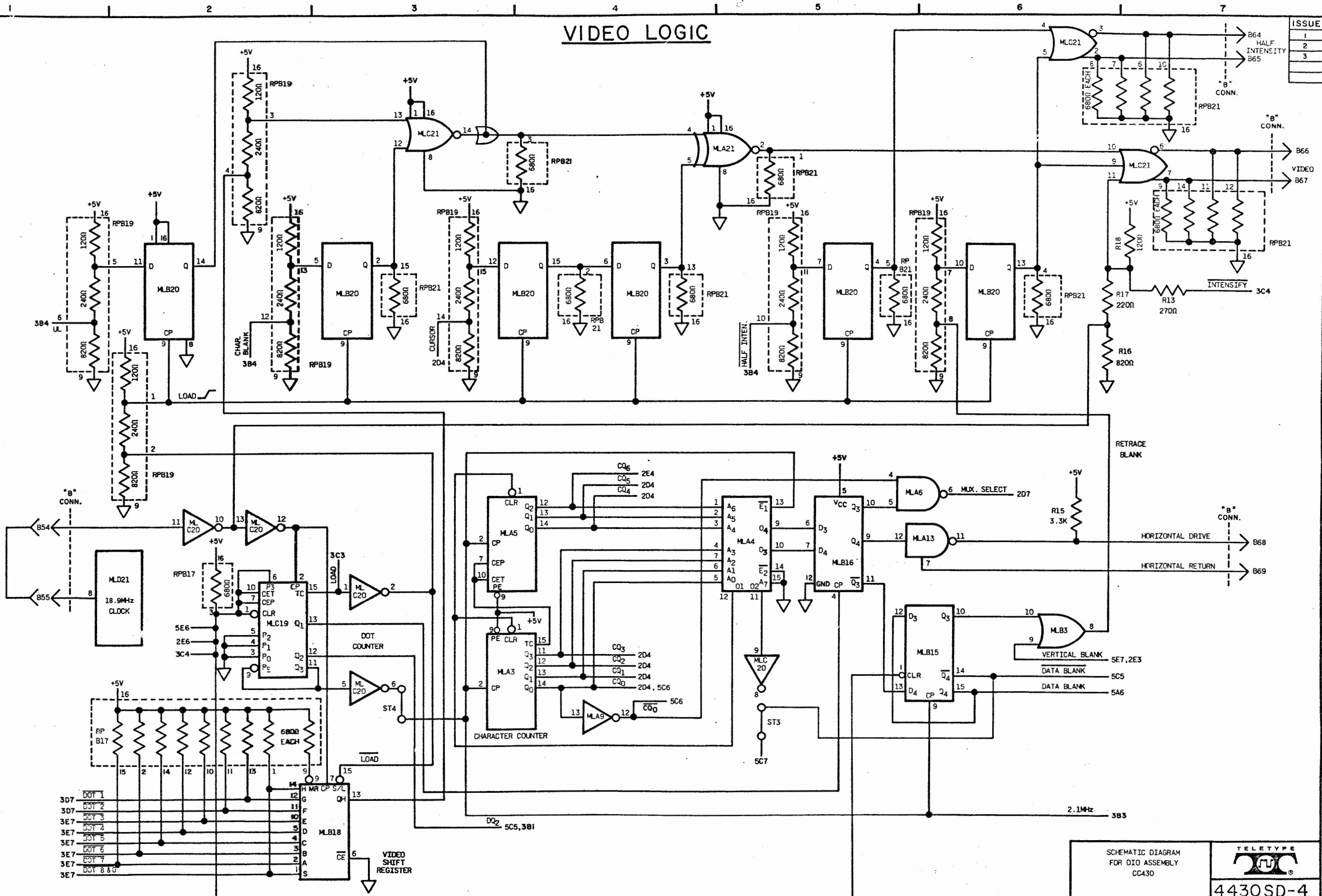
SCHEMATIC DIAGRAM
FOR
DIO ASSEMBLY
CC430



4430SD-3

94

VIDEO LOGIC

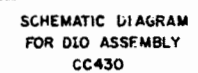


SCHEMATIC DIAGRAM
FOR DIO ASSEMBLY
CC430



4430SD-4

ISSUE
1
2
3
4
5



4430SD-50F5

SHEET INDEX

CONTENTS	SHEET NO.	ISSUE NO.																									SHEET NO.
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
SHEET INDEX, SUPPORT INFORMATION, BLOCK DIAGRAM	1	1	2	3	4																						1
FS-1 DATA/ADDRESS LOGIC	2	1	2	2	2																						2
FS-2 CONTROL LOGIC	3	1	1	2	3																						3
FS-3 MEMORY ARRAY	4	1	1	1	1																						4
FS-4 VOLTAGE AND BYPASS CIRCUITS	5	1	1	1	1																						5
TC-1 TIMING DIAGRAM	6	1	1	1	1																						6

SUPPORTING INFORMATION

CATEGORY		NO.
CIRCUIT DESCRIPTION		4464C
CIRCUIT CARD	8K	410464
	4K	410465

USE OF SHEET INDEX

WHEN CHANGES ARE MADE IN THIS DRAWING:

1. ONLY CHANGED SHEETS WILL BE REISSUED. (INCLUDING SHEET 1)
2. UNCHANGED SHEETS RETAIN EXISTING ISSUE NUMBER.

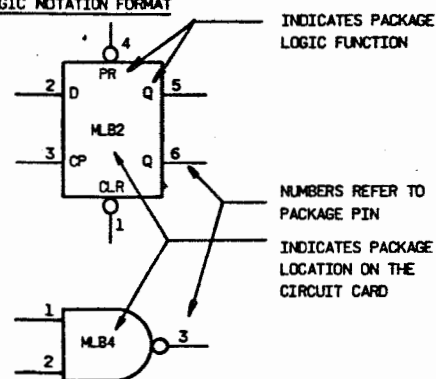
THE LAST COMPLETED COLUMN ON THE SHEET INDEX INDICATES THE LATEST ISSUE PER SHEET.

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	10-26-76	24695-R
2	4-18-77	18403
3	11-4-77	20043
4	10-30-78	15448

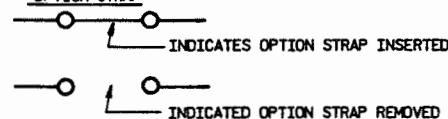
NOTES:

1. UNLESS OTHERWISE INDICATED, +5V IS APPLIED TO PIN 14 OF 14 PIN PACKAGES AND PIN 16 OF 16 PIN PACKAGES. GROUND IS APPLIED TO PIN 7 OF 14 PIN PACKAGES AND PIN 8 OF 15 PIN PACKAGES

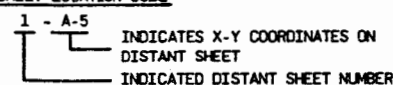
2. LOGIC NOTATION FORMAT



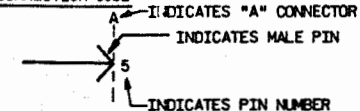
3. OPTION STRAP



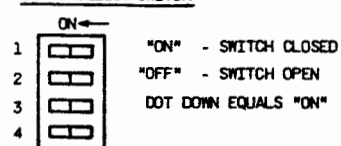
4. SHEET LOCATION CODE



5. CONNECTION CODE

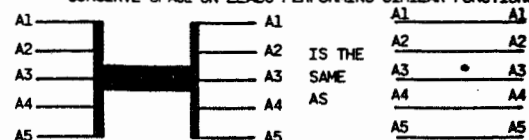


6. BOARD SELECT SWITCH



7. CABLING

THE FOLLOWING INTERCONNECTION METHOD IS USED TO CONSERVE SPACE ON LEADS PERFORMING SIMILAR FUNCTIONS



8. CONNECTOR PIN ASSIGNMENT

CONNECTOR	PIN	DESCRIPTION	LOC. ON SHEET
A	1	I/O CLK	3C1
A	3	BUS ENABLE CLK	3C1
A	5	MEM CLK	3C1
A	7	INTG IN	3C1
A	8	INTG OUT	3C1
A	15	INITIALIZE	3B1
A	19	C0	3C1
A	21	C1	3C1
A	23	C2	3C1
A	25	D/A 0	2A1
A	27	D/A 1	2A1
A	29	D/A 2	2A1
A	31	D/A 3	2A1
A	33	D/A 6	2B1
A	35	D/A 5	2B1
A	37	D/A 6	2B1
A	39	D/A 7	2C1
A	41	D/A 8	2C1
A	43	D/A 9	2C1
A	45	D/A 10	2D1
A	47	D/A 11	2D1
A	49	D/A 12	2E1
A	51	D/A 13	2E1
A	53	D/A 14	2E1
A	55	D/A 15	2E1
A	61	+5V STANDBY	5B1
A	62	-12V STANDBY	5D1
A	63	+12V STANDBY	5C1
A	68	+5V	5C1
A	69	+5V	5C1
A	70	0V	5D1
A	71	0V	5D1

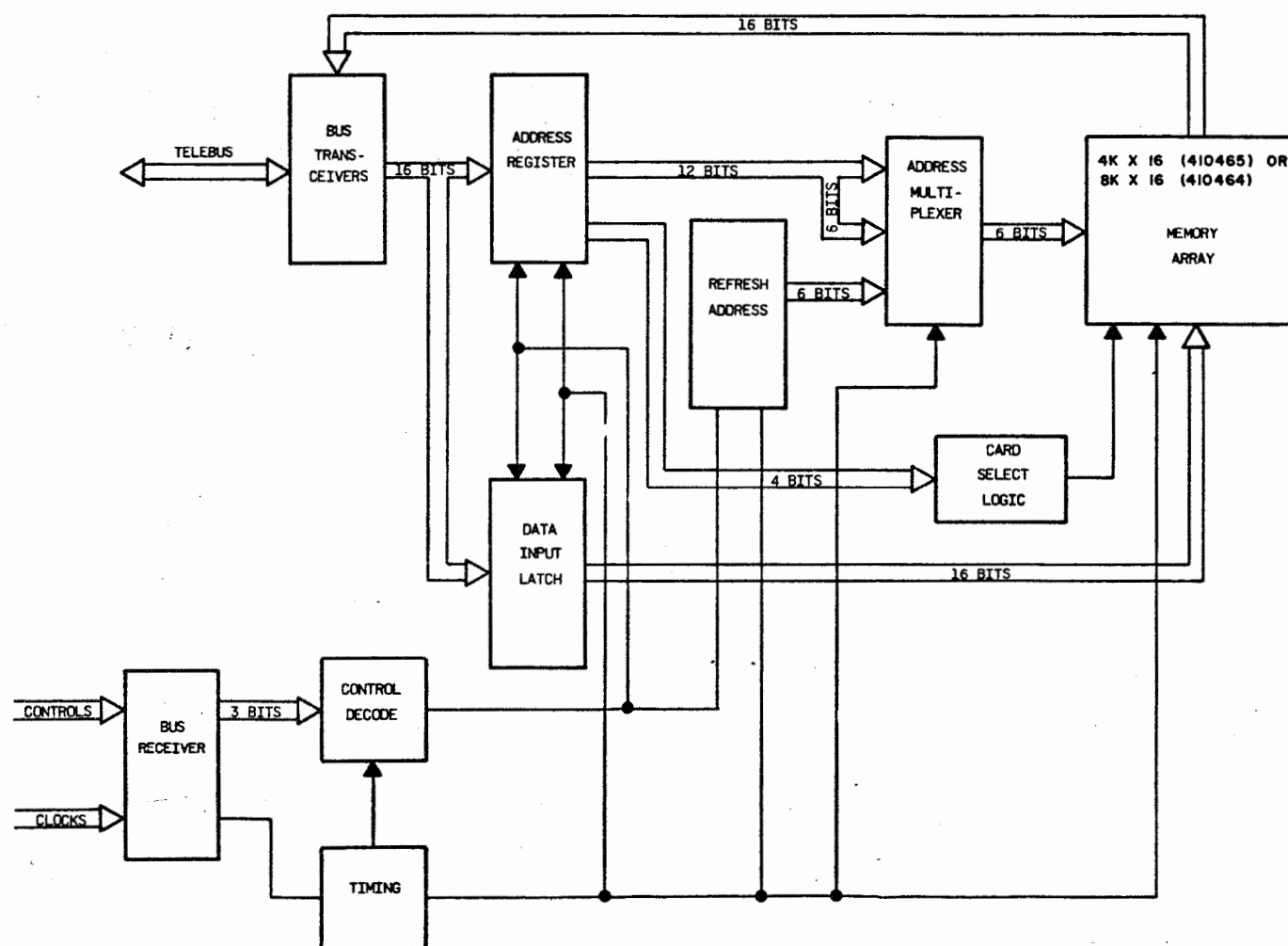
9. ALL CAPACITANCE VALUES IN MICROFARADS, ALL RESISTOR VALUES IN OHMS; UNLESS OTHERWISE SPECIFIED.

10. STANDBY VOLTAGE CODE



11. CIRCUIT CARD ISSUE 2A DELETES CONNECTION MLA4-6 TO MLA4-2 AND ADDS CONNECTION MLA4-2 TO MLA4-1, ADD CAPACITORS C54 THROUGH C57.

BLOCK DIAGRAM



SCHEMATIC DIAGRAM FOR READ/WRITE MEMORY

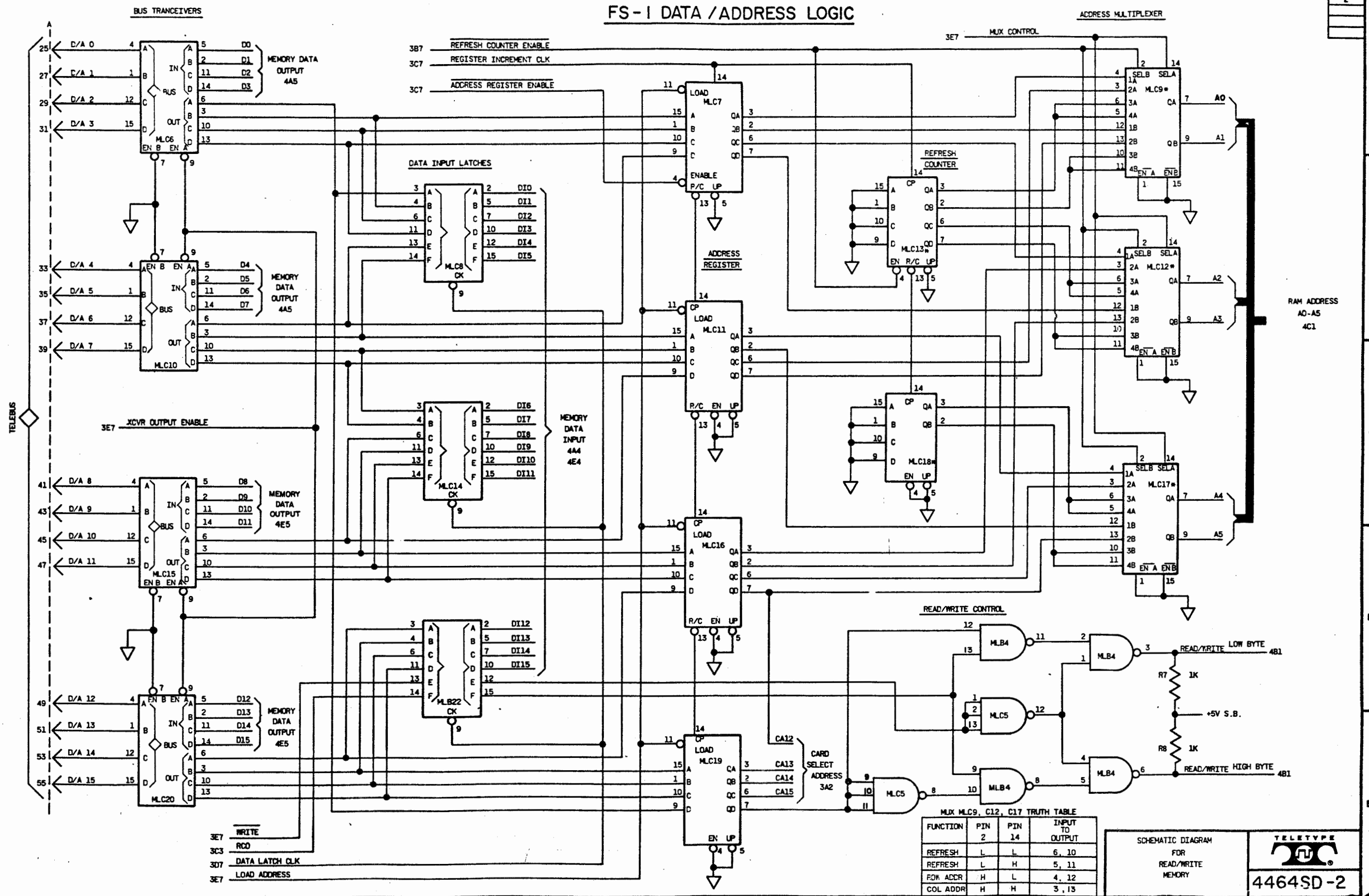
APPROVALS		
PROJ. SURV.	PROJ. DIR.	MFG. REL. COMPL.
ENGR. A.B. DSGNR.	DATE 6-24-76	
DRN	R&D FILE 6-167.172AA	
S-NUMBER		



4464SD-1

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FS - I DATA / ADDRESS LOGIC



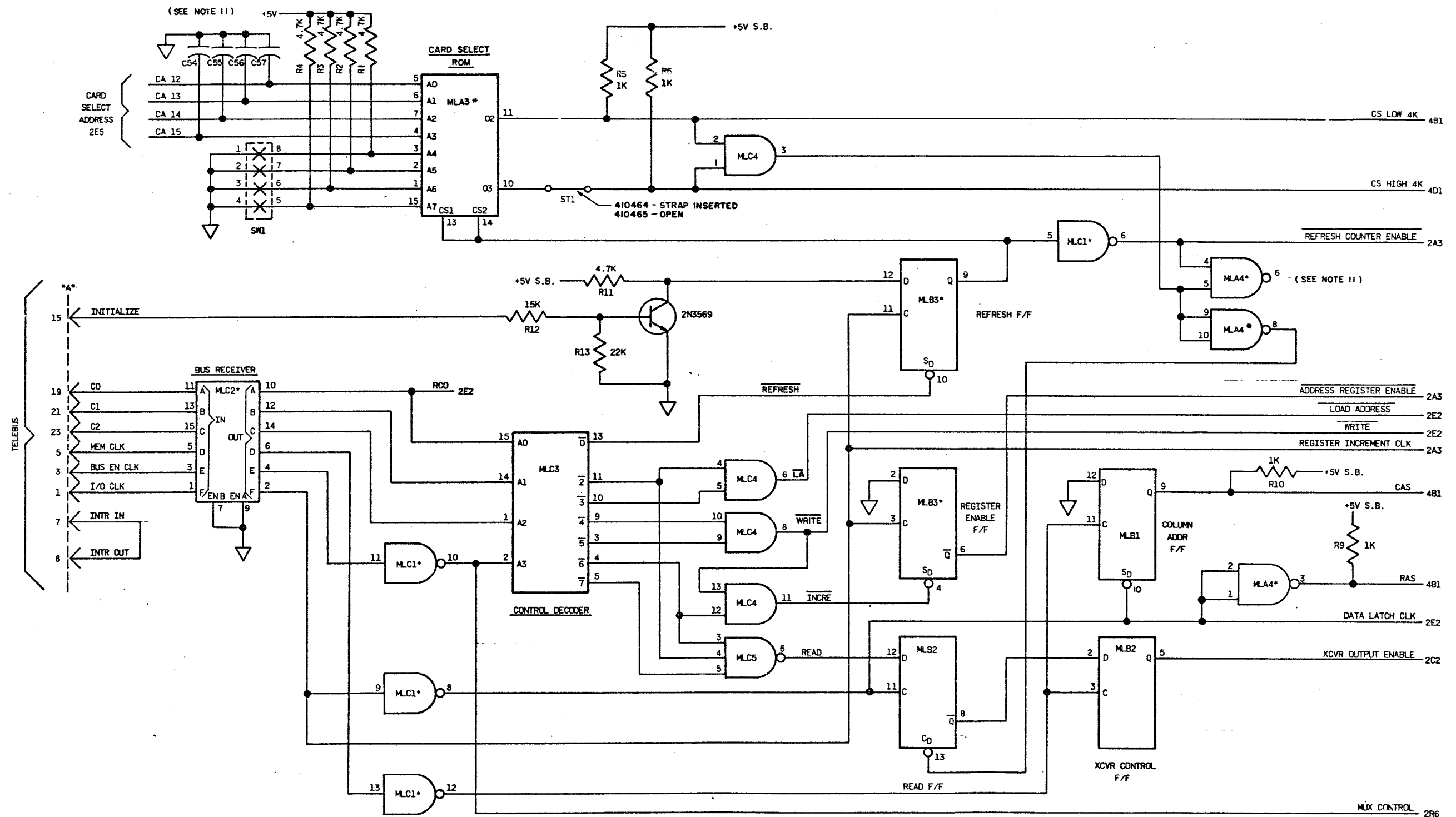
MUX MLC9, C12, C17 TRUTH TABLE

FUNCTION	PIN 2	PIN 14	INPUT TO OUTPUT
REFRESH	L	L	6, 10
REFRESH	L	H	5, 11
ROW ADDR	H	L	4, 12
COL ADDR	H	H	3, 13

SCHEMATIC DIAGRAM
FOR
READ/WRITE
MEMORY

TELETYPE
4464SD-2

FS-2 TIMING AND CONTROL LOGIC



MLC3 DECODER					
ADDRESS				OUTPUT	FUNCTION
A3	A2	A1	A0	PIN	
0	0	0	0	13	REF
0	0	0	1	12	-
0	0	1	0	11	LAR
0	0	1	1	10	LA
0	1	0	0	9	WRI
0	1	0	1	3	WBI
0	1	1	0	4	RI
0	1	1	1	5	R

SCHEMATIC DIAGRAM
FOR
READ/WRITE
MEMORY

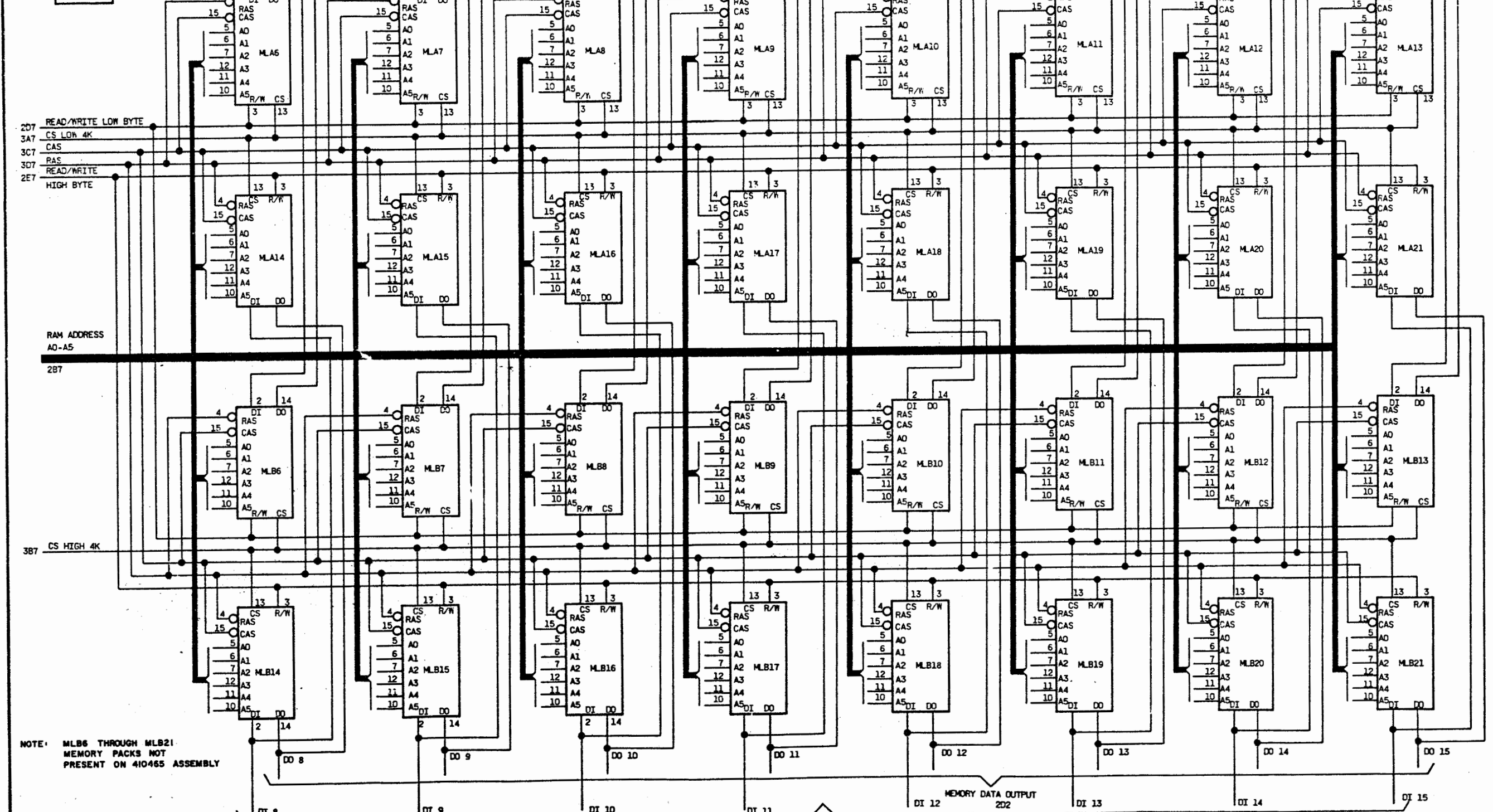
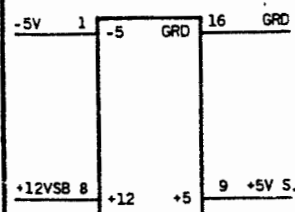


4464SD-3

FS-3 MEMORY ARRAY

ISSUE
1

POWER CONNECTIONS
ALL MEMORY PACKS

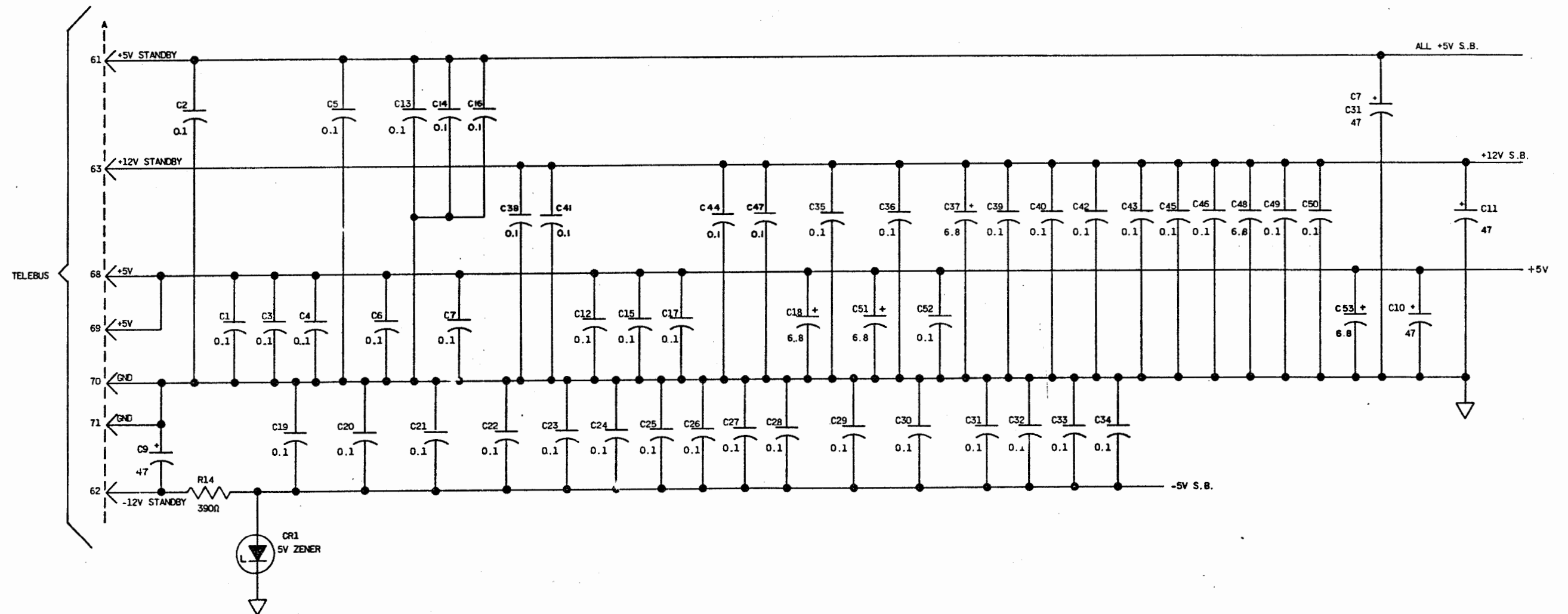


NOTE: MLB6 THROUGH MLB21
MEMORY PACKS NOT
PRESENT ON 410465 ASSEMBLY

SCHEMATIC DIAGRAM
FOR
READ/WRITE
MEMORY

TELETYPE
4464SD-4

FS-4 VOLTAGE AND BYPASS CIRCUITS



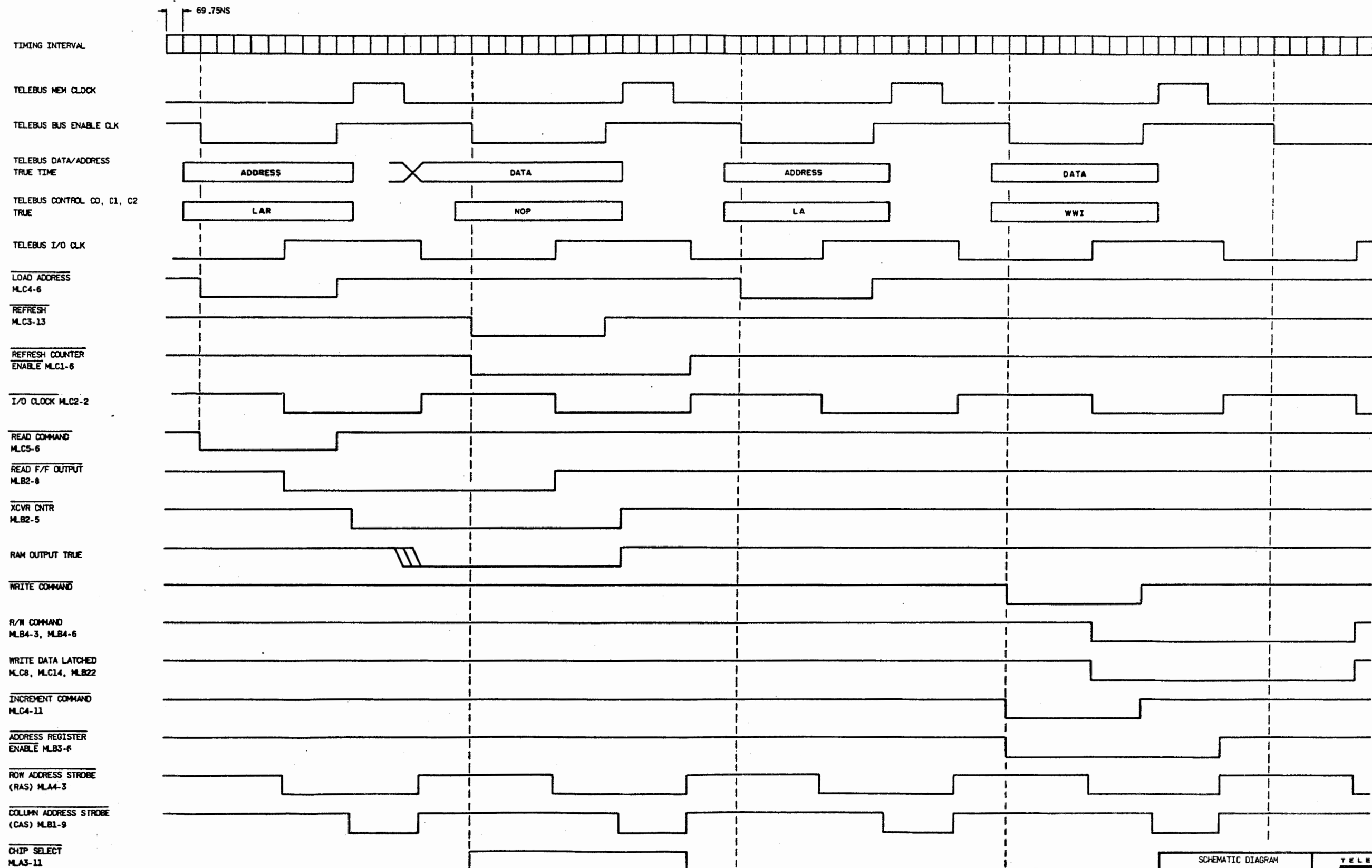
SCHEMATIC DIAGRAM
FOR
READ/WRITE MEMORY



4464SD-5

TCI TIMING DIAGRAM

ISSUE
1



SCHEMATIC DIAGRAM
FOR
READ/WRITE MEMORY



4464 SD-6

SHEET INDEX

CONTENTS	SHEET NO.	ISSUE NO.																									SHEET NO.
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
SHEET INDEX, SUPPORTING INFORMATION, BLOCK DIAGRAM	1	1	2	3																							1
FS-1 DATA/ADDRESS LOGIC	2	1	2	3																							2
FS-2 CONTROL LOGIC	3	1	2	3																							3
FS-3 ROM MEMORY ARRAY	4	1	1	1																							4
FS-4 VOLTAGE, PULL-UP, BY-PASS CIRCUITS	5	1	2	2																							5
TC-1 TIMING CHART	6	1	1	1																							6

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT CARD ASSEMBLIES	4105XX
CIRCUIT DESCRIPTION	4500CD
CIRCUIT CARD	410504
	410505

USE OF SHEET INDEX

WHEN CHANGES ARE MADE IN THIS DRAWING.

- ONLY CHANGED SHEETS WILL BE REISSUED. (INCLUDING SHEET 1)
- UNCHANGED SHEETS RETAIN EXISTING ISSUE NUMBER.

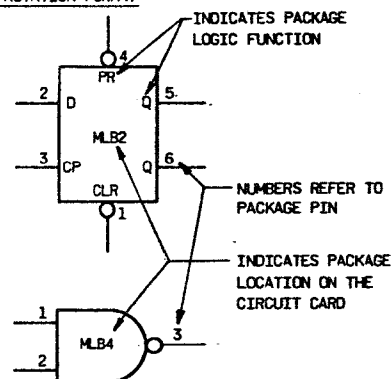
THE LAST COMPLETED COLUMN ON THE SHEET INDEX INDICATES THE LATEST ISSUE PER SHEET.

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	10-25-76	24724 R
2	2-14-79	22330
3	3-21-79	22474

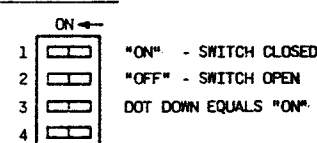
NOTES:

- UNLESS OTHERWISE INDICATED, +5V IS APPLIED TO PIN 14 OF 14 PIN PACKAGES AND PIN 16 OF 16 PIN PACKAGES. GROUND IS APPLIED TO PIN 7 OF 14 PACKAGES AND PIN 8 OF 16 PIN PACKAGES.

2. LOGIC NOTATION FORMAT

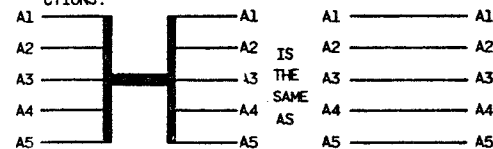


3. BOARD SELECT SWITCH

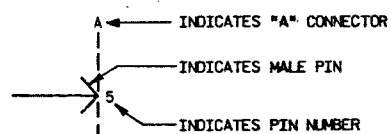


4. CABLING

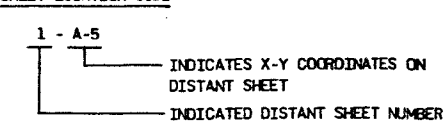
THE FOLLOWING INTERCONNECTION METHOD IS USED TO CONSERVE SPACE ON LEADS PERFORMING SIMILAR FUNCTIONS.



5. CONNECTOR CODE



6. SHEET LOCATION CODE

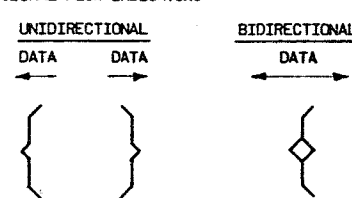


7. CONNECTOR PIN ASSIGNMENT

CONNECTOR	PIN	DESCRIPTION	LOC. ON SHEET
A	1	I/O CLK	5B2
A	3	BUS EN CK	3D1
A	5	MEM CK	3D1
A	7	INTG IN	5C2
A	8	INTG OUT	5C2
A	10	INTR	5B2
A	12	DEV B EN	5B2
A	13	DEV A EN	5B2
A	15	INITIALIZE	5B2
A	17	TRAP	5B2
A	19	C0	3D1
A	21	C1	3D1
A	23	C2	3D1
A	25	D/A 0	2A1
A	27	D/A 1	2A1
A	29	D/A 2	2A1
A	31	D/A 3	2B1
A	33	D/A 4	2B1
A	35	D/A 5	2C1
A	37	D/A 6	2C1
A	39	D/A 7	2C1
A	41	D/A 8	2C1
A	43	D/A 9	2D1
A	45	D/A 10	2D1
A	49	D/A 12	2E1
A	51	D/A 13	2E1
A	53	D/A 14	2E1
A	55	D/A 15	2E1
A	57	N/C	5A2
A	61	+5 STANDBY	5E2
A	64	-12V	5C2
A	65	-12V	5C2
A	66	+12V	5D2
A	67	+12V	5D2
A	68	+5V	5D2
A	69	+5V	5D2
A	70	GND	5D2
A	71	GND	5D2

- ALL CAPACITANCE VALUES IN MICROFARADS, ALL RESISTOR VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.

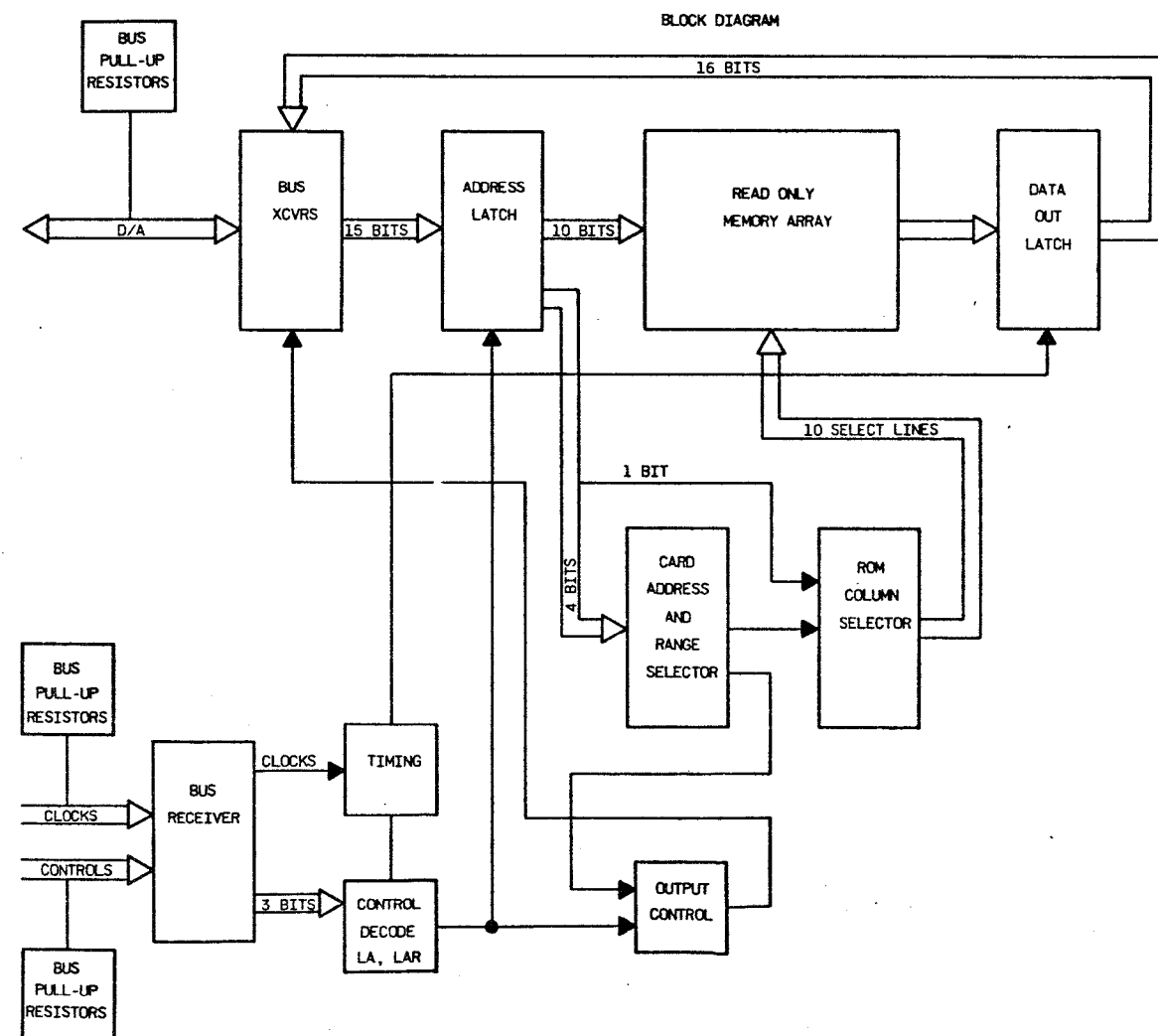
9. SIGNAL FLOW INDICATORS



- R17 THROUGH R43 ONLY PRESENT ON CIRCUIT CARDS CONSTRUCTED FROM 410504 BASE CARD.
- FULL MEMORY ARRAY SHOWN SEE SPECIFIC CARD ASSEMBLY FOR ACTUAL MEMORY CONTENT.

- ISSUE 2 OF THIS SCHEMATIC ADDS PULL UP RESISTOR RPA5-5 TO NODES MLA2-1, MLB4-1, MLB5-1 VIA AN INSULATED WIRE STRAP.

- ISSUE 3 OF THIS SCHEMATIC CHANGED THE CIRCUIT CARD ARTWORK SUCH THAT PULL UP RESISTOR RPA5-7 CONNECTS TO NODES MLA2-1, MLB1-1, MLB1-13, MLB3-1, MLB4-1, MLB5-1, MLB6-1 AND MLC7-1. PULL UP RESISTOR RPA5-5 CONNECTS TO NODE MLB1-4. THIS CHANGE MODIFIES NOTE 12.



SCHEMATIC DIAGRAM FOR EPROM

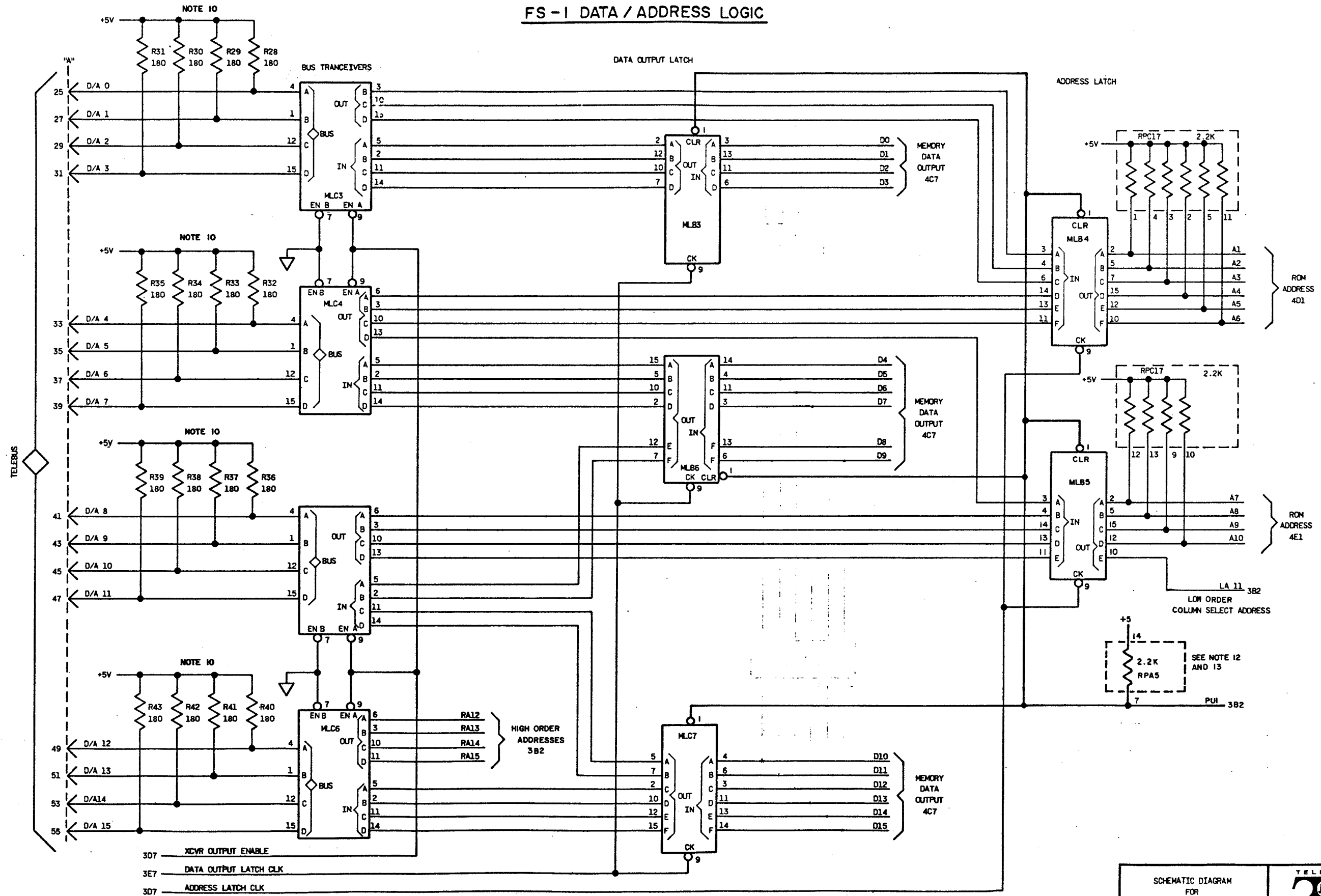
APPROVALS		
PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.
ENGR. A.B.	DSGNR.	DATE
DRN.	DATE	R&D FILE 6-167.172AA
S-NUMBER		



4500 SD-1

FS - I DATA / ADDRESS LOGIC

ISSUE
1
2
3



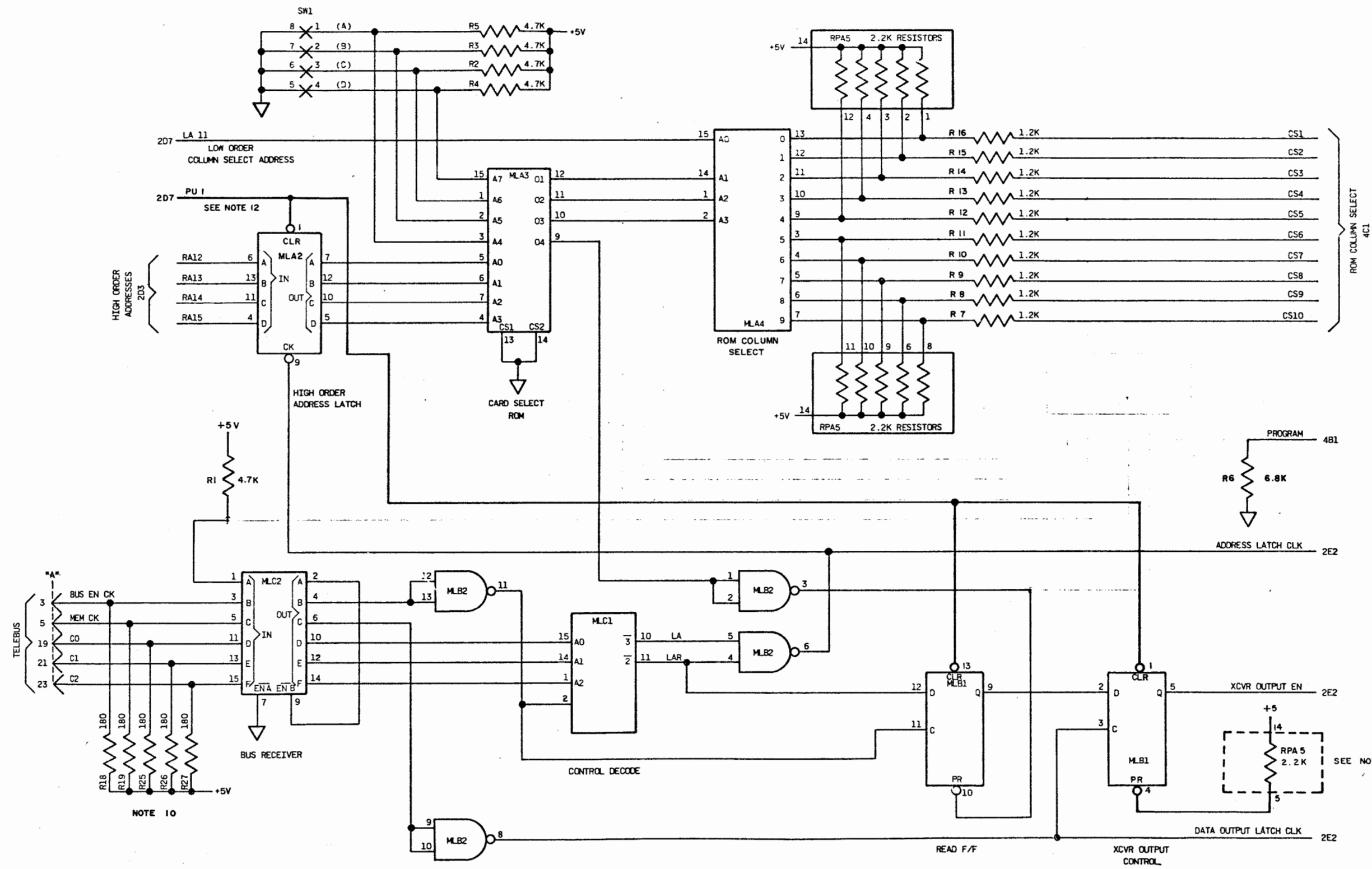
SCHEMATIC DIAGRAM
FOR
EPROM



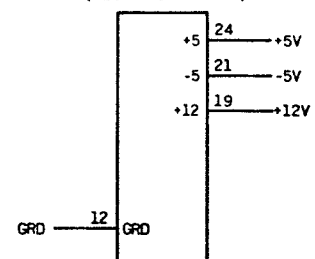
4500 SD-2

FS-2 CONTROL LOGIC

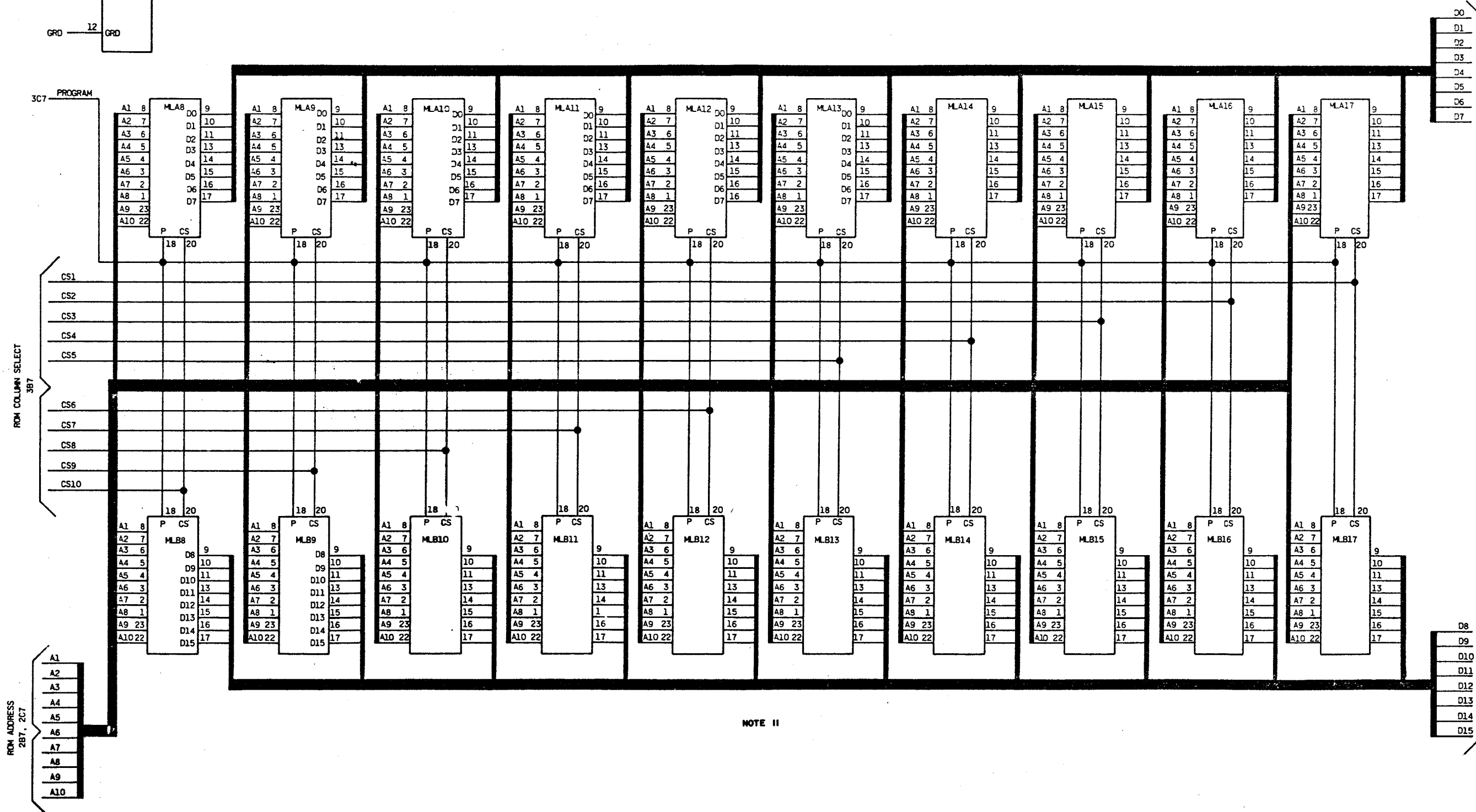
ISSUE
1
2
3



POWER CONNECTIONS
(ALL MEMORY PACKS)



FS-3 ROM MEMORY ARRAY

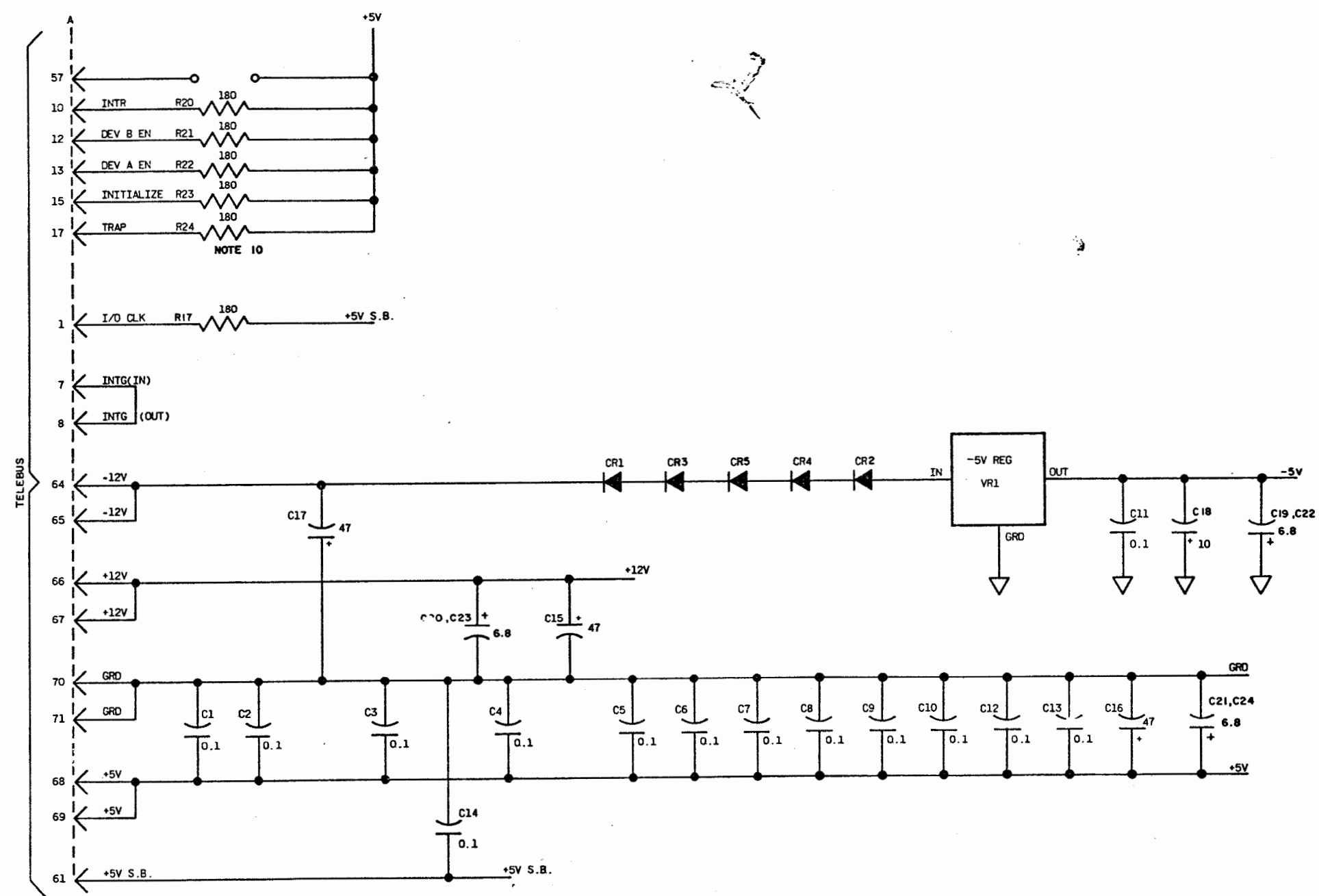


SCHEMATIC DIAGRAM
FOR
EPROM

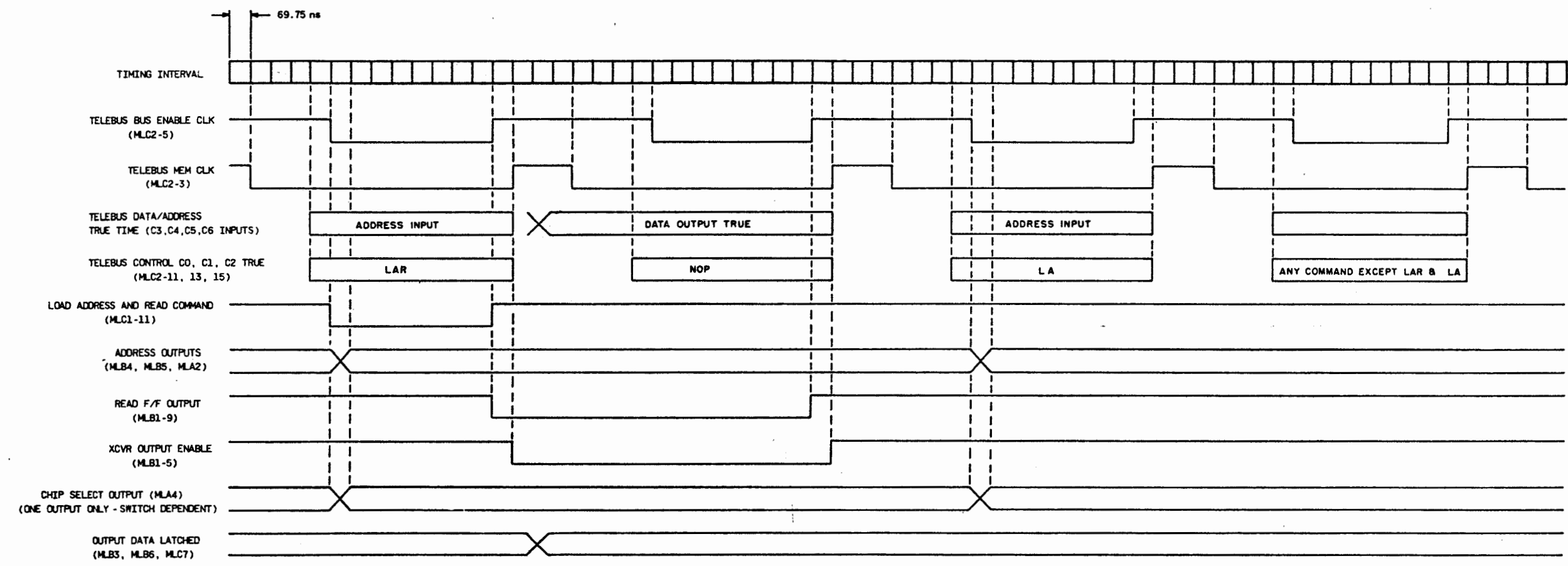


4500SD-4

FS-4 VOLTAGE, PULL UP, AND BYPASS CIRCUITS



TC-1 MEMORY TIMING CHART



SCHEMATIC DIAGRAM
FOR
EPROM



4500SD-6

CIRCUIT DESCRIPTION OF THE 410400

INSTRUCTION EXECUTIVE LOGIC/A CARD ASSEMBLY

Section I - User Information

1. General Description

1.1 The 410400 Instruction Execution Logic/A (IXL/A) Card Assembly and the 410401 Instruction Execution Logic/B (IXL/B) Card Assembly provides the logic and timing necessary to execute the instruction stream for the 40C400 Controller.

1.2 The IXL/A card assembly contains the data path logic, consisting essentially of a Bus Interface, Register File, Arithmetic and Logic Unit, and a Status Register. The controls for the logic are generated on the IXL/B Card and connected to the IXL/A Card via the "B" Connector. The IXL/A Card is connected to the Telebus via the "A" Connector.

1.3 In operation, each instruction is executed as a sequence of micro-steps. Each micro-step requires 1.116 microseconds. The sequence followed for a given instruction is dictated by the microprogram stored in the IXL/B Card. (Refer to 4401CD.) The steps for an instruction generally follow this sequence:

- (1) The instruction is fetched and stored; the Program Counter is advanced to the address for the next instruction.
- (2) The Source operand is fetched and stored in the Register File.
- (3) The Destination operand is fetched and stored in the Register File.
- (4) The arithmetic or logic operation is performed on the Source and Destination and the result is stored in the Register File.
- (5) The result is written in the Destination address.

1.4 The number of micro-steps per instruction varies from 2 to 12. During each step, the control leads from the IXL/B select the logic operation for the IXL/A Card. At the next step, a different logic operation is selected.

2. Features

2.1 The operational features of the IXL/A Card are described by the instruction set of 40C400 Controller (refer to 4401 CD).

2.2 Run Light

2.2.1 One feature unique to the IXL/A Card is the Run Light. This is a Light Emitting Diode (LED) on the left side of the card which is normally positioned to the front of the module. Each execution of the DLA instruction actuates a timer circuit which in turn energizes the Run Light for approximately 100 milliseconds. By executing the DLA instruction every 100 milliseconds during normal operation of the Controller, the Run Light appears as a continuously glowing indicator. Deviation from normal operation should cease execution of the DLA instruction with the consequent extinguishing of the Run LED. In this manner, the Run Light serves as an indicator of Controller operation.

2.2.2 Provision is made for locating the Run Light at a remote location. Pin (B68) of the IXL/A "B" Connector may be connected to another LED through the backpanel and an external cable.

2.3 Restart Function

2.3.1 A Restart Function is provided on the IXL/A Card. It permits a Restart Switch to be connected to the IXL/A via the Back Panel. Operation of the Restart Switch causes a timed active low signal on the Telebus Initialize lead similar to that provided by the Power On Reset (POR) generated by the Power Supply whenever AC Power is initially applied.

2.3.2 The condition of the Restart Switch, open or closed, is reflected in Bit 5 of the Status Register where an instruction may be used to test for the state of the switch. This permits differentiation between Initialize generated by the POR and one generated by operation of the Restart Switch. The System Power Up sequence can use this difference to either restart the user's program or branch to the System Absolute Loader.

2.3.3 Two straps may be inserted to obtain one of three modes of operation. The IXL/A Card is supplied with Strap S₂ inserted and Strap S₁, deleted.

2.3.3.1 Whenever both of the two straps are connected, Bit 5 of the Status Register is wired to a permanent "0" condition and the Restart Switch option is bypassed. Upon termination of the Initialize signal, the IXL will automatically sequence through the vector address at location 177776.

2.3.3.2 Whenever strap S₂ is inserted and S₁ is deleted, bit 5 of the Status Register is wired to a permanent "0" condition, but the Restart Switch option is effective. Each time the switch is operated, an Initialize signal will be generated causing the IXL to recycle to the Power-Up sequence through the vector address contained at location 177776.

2.3.3.3 Whenever strap S₂ is deleted and S₁ is inserted, the Restart Switch option is again effective and the Status Register Bit 5 reflects the state of the Restart Switch. Consequently, whenever an Initialize signal has caused the IXL to recycle to the Power-Up sequence, operation of the Restart Switch is required to allow the power up sequence to be completed.

2.4 Continue Switch

2.4.1 The Continue Switch is a momentary switch located at the top, left of the IXL/A Card adjacent to the Run Light. This switch is intended to be utilized by a field maintenance person during Self-Test checkout of the 40C400 Controller.

2.4.2 The Self-Test procedure allows the System Designer to vary the composition of a 40C400 Controller within the framework of the System Definition and still permit the Self-Test sequence to function without modification.

3. Supporting Information

3.1 Schematic 4400SD.

Section II - Circuit Description1. General

1.1 The 410400 Card Assembly requires +5 Volts from the power supply. The voltage drop of the power leads on the 410400 card has been held to less than 2%. The power supply system should provide the +5 Volts with sufficient tolerance to include the 2% due to card voltage drop and still provide +5 Volts $\pm 10\%$ at the supply leads of all integrated circuit packages.

1.2 Other voltages referred to in the circuit description have the following tolerances:

<u>Voltage</u>	<u>Voltage Range</u>
V_L	0.0 V. to +0.4 V.
V_H	+2.4 V. to 5.5 V.

1.3 The logic notation format is shown in 4400 SD-1.

1.4 Positive logic symbols are used in the associated schematic (4400 SD).

1.5 Signal leads are labeled with a title of the function of the signal. A line drawn over the title indicates the signal to be in a low (V_L) state when the function described by the title is active or present. A title with no line indicates the signal to be in a high (V_H) state when the function described by the title is active or present.

1.6 All Telebus signal leads have a line drawn over their titles indicating the V_L state is the active state. The Telebus logic 1 is a V_L voltage level with the logic 0 a V_H voltage level.

1.7 The IXL/A card has an "A" and a "B" Connector. Power and Telebus signal leads utilize the "A" Connector. All leads to and from the IXL/B card utilize the "B" Connector. Two leads for the Run LED Timer function are connected to the back bus via the "B" Connector. The connector notation format for the schematics is shown in 4400 SD-1.

2. Block Diagram

2.1 The IXL/A Block Diagram, shown in 4400 SD-2, depicts the functional blocks and interconnections of the IXL/A Card Assembly. Within each block is listed the Functional Schematic (FS) which provides the detailed schematic of the block.

2.2 All the functional blocks have control leads connected to the IXL/B card via the "B" Connector. Interconnection of the control leads is not shown in the Block Diagram.

2.3 The BUS INTERFACE consists of bus transceivers to receive the 16 lead Data/Address Telebus signal and to drive the Data Address (D/A 15 - D/A0) Telebus signal leads under control of the microprogram. Within the IXL/A

2.3 (Continued)

Card, the signal leads D/A 15 - D/A0 are connected to the "A" MULTIPLEXER and to the IXL/B card via the "B" Connector.

2.4 The REGISTER FILE is 16 word by 16 bit random access memory. The 16 words store the contents of the 16 registers of the IXL. During each microprogram step, data can be read from one of the registers, modified by the IXL/A logic, and written into the same register. The address selection and write control leads of the REGISTER FILE originate in the IXL/B card. The output of the REGISTER FILE can be transferred to the Data/Address signal leads of the Telebus under microprogram control; the output is also connected to the B input of the ARITHMETIC AND LOGIC UNIT.

2.5 The "A" MULTIPLEXER selects data from the ACCUMULATOR or the D/A(15) - D/A(0) signal leads and presents the data to the A input of the ARITHMETIC AND LOGIC UNIT. An integral part of the selection is the Sign Extend Multiplexer (SGNX MULTIPLEXER) used to extend the logic value of Bit 7 to Bit 8 through Bit 15.

2.6 The ARITHMETIC AND LOGIC UNIT (ALU) performs 16 arithmetic and 16 logic operations on two 16 bit words. The inputs A and B are 16 bit words; the output F is also a 16 bit word. The Carry In Multiplexer (CIN MULTIPLEXER) selects a value for the carry input from the ACCUMULATOR or the STATUS REGISTER. The ARITHMETIC AND LOGIC UNIT and the CIN MULTIPLEXER control signals are generated by the Microprogram Read Only Memory (ROM) and transmitted to the IXL/A card via the "B" Connector.

2.7 The ACCUMULATOR is a 16 bit storage register. The output (F) of the ARITHMETIC AND LOGIC UNIT is stored in the ACCUMULATOR during each V_L to V_H transition of the Accumulator Clock (ACC CLK). The ACCUMULATOR output is available in both true and inverted state.

2.8 The STATUS REGISTER is a 6 bit storage register. The values of the Status bits C,Z,N,P, and T plus the value of a microprogram flag, CNTEN, are stored in the register during each V_L to V_H transition of the ACC CLK.

2.9 The STATUS MULTIPLEXER selects values for the C,Z,N,P,T status bits from the ARITHMETIC AND LOGIC UNIT output, the ACCUMULATOR output and the STATUS REGISTER output. The STATUS MULTIPLEXER output is stored in the STATUS REGISTER. The value of the status bits are calculated once per instruction. Since the STATUS REGISTER is clocked once per microstep, the status bits value are stored by recirculating the STATUS REGISTER output through the STATUS MULTIPLEXER to the input of the register.

2.10 The RUN LED TIMER drives the RUN LED and provides the Run Timing function. A RUN IN signal in the V_L state for approximately 3 microseconds will trigger the timer. The timer provides a pulse approximately 100 milliseconds in duration. In turn, the timer actuates the RUN LED for 100 milliseconds.

3. Description of FS-1 Bus Interface and Register File

3.1 General

3.1.1 The BUS INTERFACE provides the interface for the IXL/A card to the Telebus Data/Address signal leads. Data can be received or transferred to the Telebus D/A leads under control of the OUT ENABLE lead driven by the IXL/B card.

3.1.2 The REGISTER FILE is a 16 word by 16 bit random access memory which stores the contents of the 16 IXL registers. During each microprogram step of 1.12 microseconds, data can be read from a register, modified by the data path logic, and written into the same register.

3.1.3 Refer to 4400 SD-3 for the FS-1 schematic and 4400 SD-9, -10, -11 and -12 for timing charts.

3.2 Telebus BUS INTERFACE

3.2.1 The bus transceivers MLC7, MLC5, MLC9, and MLC3 interface the IXL/A card to the Telebus signal leads D/A0 through D/A 15. Each transceiver contains 4 high input impedance receivers and 4 open collector drivers connected to provide bidirectional bus data flow.

3.2.2 To receive data from the Telebus, the transceiver drivers are disabled by a V_H state on the OUT ENABLE lead. The high impedance receivers within the transceivers amplify, invert the Telebus D/A signals, and drive the D/A0 through D/A 15 IXL/A signal leads. The D/A0 through D/A 15 signal leads drive the "A" MULTIPLEXER and the IXL/B card Instruction Register through the "B" Connector.

3.2.3 To transfer data from the IXL to the Telebus requires a V_L state on the OUT ENABLE lead. Data from the REGISTER FILE (RB0 through RB 15) is inverted by the bus transceivers and drives the Telebus D/A0 through D/A 15 signal leads. Since the receivers within the bus transceivers are always active, the Telebus signals are returned to the IXL/A card. The state of RB0 through RB 15 signal leads is reflected by the Telebus bus transceivers onto the IXL D/A0 through D/A 15 signal leads.

3.2.4 The timing cycle for the IXL/A card begins with the V_L to V_H transition of the microprogram clock and extends until the next V_L to V_H transition. If data is to be transferred from the IXL/A card to the Telebus, the OUT ENABLE signal is actuated shortly after the MICROPROGRAM CLOCK positive transition. The OUT ENABLE is activated (V_L) sufficiently in advance of BUS ENABLE to conform with the Telebus timing discipline that D/A signal leads be stable 70 nanoseconds prior to the V_H to V_L BUS ENABLE transition. Since OUT ENABLE remains activated until the next MICROPROGRAM CLOCK transition, D/A generated by the IXL/A card does remain stable for at least 70 nanoseconds beyond the V_L to V_H BUS ENABLE transition. (Refer to TC-1,-2,-3, and -4.)

3.3 REGISTER FILE

3.3.1 The REGISTER FILE is constituted from four 16 word by 4 bit read/write memories (MLC4, MLC6, MLC8, and MLC10) to form a 16 word by 16 bit storage file. The 16 registers are:

Mnemonic	Name
R0,R1,R2 R3,R4,R5,R6 R7 (SP)	General Purpose Registers General Purpose Register can act as a Stack Pointer
PC	Program Counter
SRC	Source Register
TEMP	Temporary Register
X	Register used for Store Instruction
Y,Z	Spare Register
IV	Interrupt Register
TRAP	Trap Register

3.3.2 The address of the REGISTER FILE is selected by the signal leads R0, R1, R2, and R3. The coding or state of the leads are listed and shown in 4400 SD-3. When the address leads are stable, correct data will be read out of the REGISTER FILE within 60 microseconds. The REGISTER FILE output is a V_H for a logic one and a V_L for a logic zero. The 16 output signal leads (RB0-RB 15) drive the "B" input leads of ARITHMETIC AND LOGIC UNIT and the bus drivers of BUS INTERFACE. Data can flow out of the REGISTER FILE through the BUS INTERFACE to the Telebus D/A signal leads.

3.3.3 Within one timing cycle of the IXL/A card, data is read from and written into the REGISTER FILE. Within the cycle one register address is used. At the beginning of the cycle, the REGISTER FILE is in the read mode. At the end of the cycle, Write Upper Byte (WUB) and Write Lower Byte (WLB) can be asserted. When asserted, data from the ACCUMULATOR is written into the REGISTER FILE. The WUB and WLB signals are timed to be inactive prior to the subsequent address change to the next IXL/A card cycle. Refer to TC-1,-2,-3, and -4.

3.3.4 The integrated circuit packages used for the REGISTER FILE read out the complement of the data read into the memory. The REGISTER FILE output is asserted as positive logic. To accommodate the data inversion, the complement of the data is written into the REGISTER FILE.

4. Description of FS-2 "A" Multiplexer Low Byte

4.1 General

4.1.1 The "A" Multiplexer - Low Byte selects data from the ACCUMULATOR, STATUS REGISTER or the D/A(15) - D/A(0) signal leads and presents the selected data as the low byte of the A input to the ARITHMETIC AND LOGIC UNIT. Three leads (MUX0, MUX1, and MUX2) from the IXL/B card control the selection.

4.1.2 Refer to 4400 SD-4 for the FS-2 schematic and 4400 SD-9,-10,-11 and -12 for timing charts.

4.2 "A" MULTIPLEXER - Low Byte

4.2.1 The circuit packages MLB4, MLB5, MLB6, MLB7, MLB8, MLB9, MLB10, and MLB11 make up the "A" MULTIPLEXER - Low Byte. Each package provides one signal lead of the output leads $\overline{A7}$ - $\overline{A0}$. The outputs are selected from the high or low bytes of D/A, the high or low bytes of the ACCUMULATOR output, the STATUS REGISTER output, an interrupt request signal (INTR) and the state of the RESTART SWITCH.

4.2.2 The states of the three control leads (MUX0, MUX1, and MUX2) are listed in a table in 4400 SD-4. The functions of the control states are as follows:

4.2.2.1 BUS-Data from the low byte of the bus (D/A0 through D/A7) is transferred to $\overline{A0}$ through $\overline{A7}$.

4.2.2.2 BUS SWAB SGNX - Data from the high byte of the bus input signal (D/A8 through D/A15) is transferred to $\overline{A0}$ through $\overline{A7}$.

4.2.2.3 +1 - The value +1 is transferred to the $\overline{A0}$ through $\overline{A7}$ leads (001).

4.2.2.4 -2 - The value -2 expressed in twos complement (177776g) is transferred to the output leads. For the low byte, 376g is transferred to $\overline{A0}$ through $\overline{A7}$.

4.2.2.5 ACC - Data from the ACCUMULATOR (ACC0 through ACC7), expressed in positive logic (V_L = logic 0 and V_H = logic 1), is transferred to the output signal leads $\overline{A0}$ through $\overline{A7}$.

4.2.2.6 ACC SWAB - Data from the ACCUMULATOR high byte (ACC8 through ACC15), expressed in positive logic (V_L = logic 0 and v_H = logic 1), is transferred to the output leads $\overline{A0}$ through $\overline{A7}$.

4.2.2.7 ACC - SR - Data from the ACCUMULATOR ACC1 through ACC8, expressed in a positive logic, is transferred to output leads $\overline{A0}$ through $\overline{A7}$. The ACCUMULATOR signals are shifted right one bit position, that is ACC1 becomes $\overline{A0}$ and ACC8 becomes $\overline{A7}$.

4.2.2.8 STATUS - Data from the STATUS REGISTER, the Continue Switch, RESTART SWITCH, and the INTR signal lead is transferred to the $\overline{A0}$ through $\overline{A7}$ signal leads. Status bits C, Z, N, P, are transferred to leads $\overline{A0}$ through $\overline{A3}$, INTR is transferred to lead $\overline{A4}$, the state of the RESTART Switch is transferred to lead $\overline{A5}$, and the state of the Continue Switch is transferred to lead $\overline{A6}$.

4.2.3 The "A" ARITHMETIC AND LOGIC UNIT input requires active low logic levels, that is V_L equals a logic 1 and V_H equals a logic 0. The "A" MULTIPLEXER utilizes logic packages capable of providing the inverse of the output. The output pins of MLB4, MLB5, MLB6, MLB7, MLB8, MLB9, MLB10 and MLB11 provide the selected signal in active low logic levels, suitable for the "A" input of the ALU. The output $\overline{A7}$ is provided in both normal and inverted logic form.

4.2.4 The V_H input signals to the "A" MULTIPLEXER are derived from the resistor R7 connected to the +5 Volt Supply. The V_L input signals are derived by connecting the inputs to GROUND.

4.2.5 The states of the control leads are changed at the V_L to V_H transition of the MICROPROGRAM CLOCK and are stable approximately 200 nanoseconds after the transition.

5. Description of FS-3 "A" Multiplexer - High Byte and SGNX Multiplexer

5.1 General

5.1.1 The "A" MULTIPLEXER - High Byte selects data from the D/A signal leads, the ACCUMULATOR output signal leads, and the output of the SGNX MULTIPLEXER and presents the selected data as the high byte input "A" of the ARITHMETIC AND LOGIC UNIT (ALU). The states of two signal leads (MUX3 and MUX4) control the selection of the "A" MULTIPLEXER - High Byte.

5.1.2 To minimize the "A" MULTIPLEXER logic, another level of selection is provided to obtain the logic literals D8 through D15. A signal (MUX2) from the IXL/B card controls the selection of the output from either the D/A leads or the ACCUMULATOR output leads.

5.1.3 To handle data in byte form requires the sign extend logic operation. The sign bit of a byte (Bit 7) is replicated in Bits 8 through 15 to convert a byte into a word. Once in word form, the data can be processed by the word oriented IXL data path. The SGNX MULTIPLEXER provides the bit (SGNX) to be replicated. The SGNX signal lead is connected to the "A" MULTIPLEXER Bit 8 through 15 inputs. The state of the leads CYCTRL0 and CYCTRL1 control the selection of the SGNX MULTIPLEXER.

5.1.4 Refer to 4400 SD-5 for the FS-2 schematic and 4400 SD-9,-10,-11 and -12 for the timing charts.

5.2 "A" MULTIPLEXER - High Byte

5.2.1 The circuit packages MLB2, MLB3, MLB12 and MLB13 make up the "A" MULTIPLEXER - High Byte. The outputs selected are the low byte output of the ACCUMULATOR, the output of the SGNX MULTIPLEXER, and the D8 through D15 output leads from MLB1 and MLB14.

5.2.2 The integrated circuit packages MLB1 and MLB14 provide an additional level of selection. The outputs D8 through D15 are selected from D/A8 through D/A15 signal leads and the output of the ACCUMULATOR ACC8 through ACC15. Signal MUX2, a signal from the IXL/B card, controls the selection of the MLB1 and MLB14 multiplexer.

5.2.3 The states of the control levels, MUX2, MUX3 and MUX4, are listed as a table in 4400 SD-5. The functions of the control states are as follows:

5.2.3.1 BUS - Data from the high byte of the Telebus input (D/A8 - D/A15) is selected as D8 through D15 and is again selected and transferred through "A" MULTIPLEXER - High Byte to the A8 through A15 signal leads.

5.2.3.2 BUS SEX - The output of the SGNX MULTIPLEXER, SGNX, is transferred to the "A" MULTIPLEXER output A8 through A15. The total effect of the "A" MULTIPLEXER is to transfer the low byte of Telebus input data D/A0 through D/A7 and convert the byte to a word by extending D/A7 into D/A8 through D/A15.

5.2.3.3 BUS SWAB SEX - The output of the "A" MULTIPLEXER - High Byte is the output of the SGNX MULTIPLEXER. The output of the "A" MULTIPLEXER - Low Byte is the high byte of the D/A signal. The net effect of the combined action of swab and sign extend is to right justify the D/A high byte and convert the justified byte to a word.

5.2.3.4 ACC - Data from the ACCUMULATOR, expressed in positive logic, is selected by MLB1 and MLB14 multiplexers and by the "A" MULTIPLEXER - High Byte and transferred to the output signal leads A8 through A15.

5.2.3.5 ACC SEX - Data from the SGN MULTIPLEXER, SGNX, is transferred to the "A" MULTIPLEXER outputs A8 through A15.

5.2.3.6 ACC SWAB - Data from the ACCUMULATOR, ACC0 through ACC8, is transferred to the "A" MULTIPLEXER - High Byte A8 - A15.

5.2.3.7 ACC - SR - Data from the ACCUMULATOR is shifted right one bit position and transferred to the output. The ACCUMULATOR data A9 through A15 is first selected by the multiplexers MLB1 and MLB14 and transferred to the "A" MULTIPLEXER - High Byte via the data leads D9 through D15. When shifted and transferred through the "A" MULTIPLEXER - High Byte A8 equals ACC9, A9 equals ACC10, up to A14 equals ACC15. The output of the STATUS REGISTER, C, is transferred through the MLB3 to become output A15.

5.2.3.8 STATUS - The output of the "A" MULTIPLEXER - High Byte is set to a positive logic 0 (V_L). The "A" MULTIPLEXER - Low Byte is set to transfer the STATUS to A0 through A6 and a logic 0 (V_L) to A7. The SGNX MULTIPLEXER transfers the signal A7 as its output SGNX. In turn SGNX is replicated and transferred through the "A" MULTIPLEXER - High Byte outputs A8 through A15.

5.2.3.9 +1 - The output of the "A" MULTIPLEXER is selected to present +1. The high byte of the output is generated by selection of bit A7 of the low byte as SGNX by the SGNX MULTIPLEXER. In turn the signal SGNX is replicated and transferred to the "A" MULTIPLEXER output A8 through A15.

5.2.3.10 -2 - The output of the "A" MULTIPLEXER is selected to present -2, in two's complement, to its output (A15 - A0 = 1777768). The high byte A15 - A8 is formed by replicating Bit A7 in Bits A8 through A15.

5.2.4 The "A" input to the ARITHMETIC AND LOGIC UNIT requires data in an active low logic form, that is V_L = logic 1 and V_H = logic 0. The circuit packages comprising the "A" MULTIPLEXER - High Byte, MLB2, MLB3, MLB11 and MLB12 provide the output in true and inverted form. The A8 through A15 signals are derived from the inverted output to drive input "A" with active low logic data.

5.2.5 The state of the "A" MULTIPLEXER - High Byte controls (MUX2, MUX3, and MUX4) is changed once per MICROPROGRAM CLK cycle. At each V_L to V_H transition of the MICROPROGRAM CLOCK, the state of the controls is changed and becomes stable 200 nanoseconds later.

5.3 SGNX MULTIPLEXER

5.3.1 One of the four input multiplexers of circuit package MLC2 serves as the SGNX MULTIPLEXER. The inputs are A7 and Bit C of the Status. Signals CYCTRL0 and CYCTRL1, generated on the IXL/B card control the selection.

5.3.2 The states of the control leads are listed in a table in 4400 SD-5. The functions of the control states are as follows:

5.3.2.1 A7 - The output of the "A" MULTIPLEXER, Bit A7, is selected as the output SGNX.

5.3.2.2 C - The C bit of the STATUS REGISTER is selected as the output SGNX.

5.3.3 The signal SGNX is of active high logic polarity, that is V_H = logic 1 and V_L = logic 0.

5.3.4 The SGNX MULTIPLEXER control leads change state with each V_L to V_H transition of MICROPROGRAM CLOCK. The state of the control leads becomes stable within 200 nanoseconds after the transition.

6. Description of FS-4 Arithmetic and Logic Unit, the Accumulator and the Carry In Multiplexer

6.1 General

6.1.1 Functional Schematic Four depicts the detailed logic of the ARITHMETIC AND LOGIC UNIT, the ACCUMULATOR, and the CIN MULTIPLEXER; these logic blocks form the core of the IXL data path. The ARITHMETIC AND LOGIC UNIT performs the logic or arithmetic operations on data. The ACCUMULATOR stores the ALU output in a 16 bit storage register. The CIN MULTIPLEXER selects the carry signal for the ongoing logic or arithmetic operation.

6.1.2 The ARITHMETIC AND LOGIC UNIT performs 16 logic and 16 arithmetic operations on two 16 bit inputs, $\bar{A}$ and B. The output is 16 bits, F.

6.1.3 The ACCUMULATOR is a 16 bit storage register. Data is stored during each V_L to V_H transition of ACCUMULATOR CLOCK.

6.1.4 The CIN MULTIPLEXER provides a logic signal CIN as the carry input for the ALU logic and arithmetic operations.

6.1.5 Refer to 4400 SD-6 for the FS-4 schematic and 4400 SD-9, -10, -11 and -12 for timing charts.

6.2 ARITHMETIC AND LOGIC UNIT

6.2.1 The ARITHMETIC AND LOGIC UNIT (ALU) consists of the MLA5, MLA7, MLA8, and MLA10 integrated circuit packages. The ALU operates on two 16 bit word inputs, A and B. Input A is expressed in active low form (V_L = logic 1 and V_H = logic 0) while input B is expressed as active high logic levels (V_H = logic 1 and V_L = logic 0). The output, F, is a 16 bit word in active low logic levels (V_L = logic 1 and V_H = logic 0).

6.2.2 The ALU has one additional data input, CIN, which provides a carry signal for arithmetic operations. The CIN should have V_H = logic 1 and V_L = logic 0.

6.2.3 In addition to the output F, the ALU also provides the CALU and A = B signals. The CALU signal is the resulting carry out of an arithmetic operation with V_H = logic 1 and V_L = logic 0.

6.2.4 The ALU output signal A = B is used to detect the zero condition of the output F. Each integrated circuit package comprising the ALU contains a four input AND gate. The inputs are the F signals and the output is an open collector. Connecting the four open collector outputs A = B forms a 16 input AND gate. For F = 0, each F signal is V_H , and the A = B ALU signal is V_H .

6.2.5 Five signal leads, generated on the IXL/B card and connected via the "B" connector, control the ALU. The signals (S0, S1, S2, S3, and M) voltage levels and the resulting ALU operations are listed in the table in 4400 SD-6. The table of ALU operations lists the possible operations regardless of the logic polarity of the inputs or outputs.

6.2.6 The table of ALU operations lists 32 possible arithmetic and logic operations. Only the following operations are used for the IXL:

6.2.6.1 A - The output F equals the input. For each bit of A in the V_L voltage state, the corresponding F bit is in the V_L state where V_L = logic 1 for both F and H.

6.2.6.2 A + CIN - The output of the ALU equals the value of A summed with the value of CIN.

6.2.6.3 A $\wedge$ $\bar{B}$ - The ALU output equals the product of the A input and the complement or inverse of the B input. To demonstrate the difference in voltage logic levels, the truth table for each bit of the output is presented:

$\bar{A}$	B	F
$V_H = 0$	$V_L = 0$	$V_H = 0$
$V_H = 0$	$V_H = 1$	$V_H = 0$
$V_L = 1$	$V_L = 0$	$V_L = 1$
$V_L = 1$	$V_H = 1$	$V_H = 0$

6.2.6.4 A $\wedge$ B - The ALU output is the product of the A and B input signals.

6.2.6.5 0 - The ALU output is 0; that is all Bits of F are V_H voltage level.

6.2.6.6 A + A + CIN - The ALU output is the value of A summed to itself and the value CIN.

6.2.6.7 A - B - $\overline{\text{CIN}}$ - The output F equals the value of A minus B minus $\overline{\text{CIN}}$ (the inverse of CIN).

6.2.6.8 $\overline{A \vee B}$ - The output F is the inverse of the logic product of A or B.

6.2.6.9 A $\vee$ B - The output F is the logic product of A or B.

6.2.6.10 A ∇ B - The output F is the logic product of A exclusive or B.

6.2.6.11 A + B + CIN - The output F is the arithmetic sum of A plus B plus CIN.

6.2.6.12 B - The output F equals the value of the B input.

6.2.6.13 $\bar{A} \wedge B$ - The output F is the logic product of the inverse of A and B.

6.2.6.14 $\bar{A}$ - The output F equals the inverse of A.

6.2.6.15 A - $\overline{\text{CIN}}$ - The output F is the result of A minus CIN.

6.2.7 All arithmetic and logic operations are binary. Subtraction is performed by forming the two's complement of the subtrahend and summing the result to minuend.

6.2.8 The state of the ALU control leads is changed at every V_L to V_H transition of the MICROPROGRAM CLOCK and stabilizes within 200 nanoseconds of the transition. The settling time for the ALU output is dependent upon the arrival times of the inputs. The timing charts TC-1, TC-2, TC-3 and TC-4 present the different settling and arrival times the ALU in operation for four steps of the microprogram.

6.3 ACCUMULATOR

6.3.1 The ACCUMULATOR is a 16 bit word storage register composed of 16 "D" type flip-flops. Data at the input is stored and transferred with each V_L to V_H transition of ACCUMULATOR CLOCK.

6.3.2 The ACCUMULATOR provides the literal in true or complement. $\overline{ACC0}$ through $\overline{ACC15}$ signals are V_L for a logic 1 and V_H for a logic 0. The outputs $ACC0$ through $ACC15$ signals are V_H for a logic 1 and V_L for a logic 0.

6.3.3 The integrated circuit packages MIA3, MIA4, MIA11, and MIA12 comprise the ACCUMULATOR. Each circuit package contains 4 "D" type flip-flops which are positive edge clocked.

6.3.4 The state of the ALU F output, which is also the ACCUMULATOR input, is stored with each positive (V_L to V_H) transition of the ACCUMULATOR CLOCK. The ACCUMULATOR CLOCK is generated in the IXL/B card and connected via pin B38 to the IXL/A card. The positive transition of ACCUMULATOR CLOCK normally occurs 837 nanoseconds after positive transition of the MICROPROGRAM CLOCK. The exception is the microstep calling for the Read from Device (RDV). If one of the Telebus signal leads DEVICE A ENABLE or DEVICE B ENABLE is actuated, the microprogram tep for RDV is extended to 2.24 microseconds, as shown in TC1 and TC2. For this case, the ACCUMULATOR CLOCK occurs 1.95 microseconds after the positive transition of the MICROPROGRAM CLOCK. The "stretching" of the RDV microstep allows the device on the Telebus sufficient time to place data on the Telebus.

6.4 CARRY IN MULTIPLEXER

6.4.1 The CARRY IN MULTIPLEXER consists of one of the four input multiplexers of MLC2. Signal leads CYCTRL0 and CYCTRL1, derived from the IXL/B card through pins B37 and B38 control the selection of the CIN MULTIPLEXER.

6.4.2 The states of the control leads are listed in a table in 4400 SD-6. The states description follows:

6.4.2.1 0 - The output of the CIN MULTIPLEXER is set to V_L = logic 0.

6.4.2.2 1 - The output of the CIN MULTIPLEXER is set to V_H = logic 1.

6.4.2.3 C STAT - The output of the CIN MULTIPLEXER is equal to bit C of the STATUS REGISTER.

6.4.2.4 ACC15 - The output is equal to Bit 15 of the ACCUMULATOR output.

7. Description of FS-5 Status Multiplexer, Status Register and Run LED Timer

7.1 General

7.1.1 Functional Schematic Five depicts the Status Multiplexer, the Status Register, and the Run LED Timer. The IXL Status Register contains information on the current state of the IXL. The Status consists of the N, Z, C, and P bits plus the status of the INTR signal, the condition of the Restart Switch and the condition of the Continue Switch.

7.1.2 The STATUS REGISTER maintains the N, Z, C, and P bits as calculated once per instruction cycle. The data is maintained by recirculating the STATUS REGISTER output through the STATUS MULTIPLEXER back into the STATUS REGISTER. The STATUS REGISTER is clocked once per MICROPROGRAM CYCLE with each V_L to V_H transition of the ACCUMULATOR CLOCK.

7.1.3 The STATUS MULTIPLEXER selects the values for the STATUS under control of the STAT CTRL 0, STAT CTRL1, STAT CTRL2, STAT CTRL3, SEQ CTRL, and the BYTE signals derived from the IXL/B card. All STATUS bits including the INTR, Restart Switch, and Continue Switch Conditions are selected by the STATUS MULTIPLEXER.

7.1.4 The RUN LED TIMER is an analog timer which drives the RUN LED. When pulsed by a pulse of 3 microseconds or longer, the TIMER powers the RUN LED for approximately 100 milliseconds.

7.1.5 Refer to 4400 SD-7 for Functional Schematic Five and 4400 SD-9, -10, -11, and -12 for the timing charts.

7.2 STATUS REGISTER

7.2.1 The STATUS REGISTER is a storage register composed of 5 "D" type flip-flops of the integrated circuit package MLC11. The sixth "D" type flip-flop stores the Count Enable bit (CNTEN); this bit can be considered a status bit for the microprogram and is not available for program use.

7.2.2 The inputs to the STATUS REGISTER are the outputs of the STATUS MULTIPLEXER. The outputs C, Z, N, P, and T are connected to the "A" MULTIPLEXER - Low Byte, the STATUS MULTIPLEXER, the SGNX MULTIPLEXER, and to the IXL/B card via connector pins B47, B48, B49, B52, and B57. The output signal CNT EN is connected to IXL/B through connector pin B35.

7.2.3 Data is stored in the STATUS REGISTER during each V_L to V_H transition of ACCUMULATOR CLOCK.

7.3 STATUS MULTIPLEXER

7.3.1 Integrated circuit packages MLA14, MLC11, MLC13 and MLC14 comprise the STATUS MULTIPLEXER. The STATUS MULTIPLEXER selects values for the C, Z, N, P, T, and CNT EN Status bits from the ALU outputs, F, C ALU, and A = B, and from the STATUS REGISTER outputs.

7.3.2 The selection of a value for the N bit involves another multiplexer within the MLC14 circuit package. The output of the multiplexer is N ALU. The control leads are Byte and SEQ CTRL, both derived from the IXL/B card through connector pins B39 and B9. The function of this multiplexer is to select the value of N from F7 for a byte operation and from F15 for a word operation. The signal N ALU is connected the input of the STATUS MULTIPLEXER.

7.3.3 The states of the STATUS MULTIPLEXER control leads are listed in the table in 4400 SD-7. The function of each state is as follows:

7.3.3.1 XFR - The XFR is used to calculate the status for the Move, Bit Test, Bit Clear, Bit Set, Exclusive Or, Clear, One's Complement, Increment, Decrement, Test, and Exchange Bytes instructions. Status list N is the value of F7 or F15 depending on word or byte operation. The Z bit is derived from the A = B output of the ALU. The status bits P and T remain unchanged by recirculating the STATUS REGISTER outputs P and T through the STATUS MULTIPLEXER back to the inputs of the STATUS REGISTER.

7.3.3.2 SUB - The SUB state is used to calculate the status for the Subtract and Compare instructions. Status bit N is set to the value of signal F7 or F15, dependent on word or byte instruction. Status bit Z is set to the value of the A = B output of the ALU. Status bit C is set to CALU, the inverse of the carry out from the ALU. Status bits P and T remain unchanged by a recirculation of the STATUS REGISTER outputs through the STATUS MULTIPLEXER back to the inputs of the STATUS REGISTER.

7.3.3.3 NOP (RECIRCULATE) - The NOP state is used to maintain the Status from the previous microstep. Status bits C, Z, N, P, and T remain unchanged by a recirculation of the STATUS REGISTER output through the STATUS MULTIPLEXER back to the STATUS REGISTER INPUTS. The next ACCUMULATOR CLOCK V_L to V_H transition will restore the Status bits into the STATUS REGISTER.

7.3.3.4 ADD - The ADD state is used to calculate the status of the ADD, Arithmetic Shift Left, and Rotate Left instructions. Status bit N is set to the value of F7 or F15, dependent on word or byte instruction. Status bit Z is set to value of the A = B output of the ALU. Status bit C is set to value of the CALU output of the ALU. Status bits P and T remain unchanged by the recirculation of the STATUS REGISTER outputs back to the STATUS REGISTER INPUTS.

7.3.3.5 SHR - The SHR state is used to calculate the status of the Arithmetic Shift Right, and Rotate Right instructions. Status bit N is set to F7 or F15 dependent on word or byte instruction. Status bit Z is set to the value of the A = B output of the ALU. Status bit C is set to the output of the ACCUMULATOR, ACC0. Status bits P and T are maintained by recirculation of the P and T bits of the STATUS REGISTER.

7.3.3.6 BUS - The BUS state is used to transfer data from the data path to the STATUS REGISTER. Data from the Telebus or REGISTER FILE is propagated through the ALU and into the STATUS MULTIPLEXER. In turn, the new data is clocked into the REGISTER. ALU outputs F0, F1, F7 and F3 are selected by the STATUS MULTIPLEXER and stored as STATUS REGISTER bit P, C, Z, and N. Status bit T is maintained by recirculation of the STATUS REGISTER output.

7.3.3.7 CLEAR T - The CLEAR T state is used to clear the T bit of the STATUS REGISTER. The other bits of the STATUS REGISTER are maintained by recirculation of the STATUS REGISTER outputs. When cleared, the T bit is V_L .

7.3.3.8 SET T - The SET T state is used to set the T bit of the STATUS REGISTER and maintain the other bits. Bits C, Z, N, and P are restored by recirculation of the STATUS REGISTER outputs. The T bit is set or recleared by equating T to the value of the STAT CTRL0 signal in the STATUS MULTIPLEXER.

7.3.4 The control leads STAT CTRL0, STAT CTRL1, STAT CTRL2, STAT CTRL3, SEQ CTRL0, and Byte are changed once per MICROPROGRAM CLOCK cycle. The control signals begin to change value or state at the V_L to V_H transition of the MP CLK and become stable within 200 nanoseconds. The STATUS MULTIPLEXER outputs become stable prior to each V_L to V_H transition of ACC CLK.

7.4 RUN LED TIMER

7.4.1 The RUN LED TIMER is an analog timer, MLA2, with resistor R1 and capacitor C1 as the timing components. The input is the RUN (IN) signal; the output is the RUN (OUT) signal and the RUN LED.

7.4.2 A pulse of three microseconds or longer of V_L level applied to the RUN (IN) lead will trigger the timing circuit. The timer output, MLA2(3) rises to V_H for approximately 100 milliseconds, actuating the RUN LED and driving RUN (OUT) to V_H .

SHEET INDEX AND ISSUE CONTROL

4401CD

CIRCUIT DESCRIPTION OF THE
INSTRUCTION EXECUTION LOGIC/B (IXL/B)
(410401)

Sheet 1

REVISIONS

ISSUE	DATE	AUTH. NO.
1	3-18-75	23863R

SHEET NUMBER

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
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SHEET ISSUE NUMBER

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.
<i>SPR</i>	<i>33</i>	<i>DM</i>

ENG. SA/GH

DATE 2/28/75

R&D FILE NO.
6-167.172AA

DSGNR.

DRN.

S-NUMBER

E-NUMBER



4401CD

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SHEET INDEX AND ISSUE CONTROL

4401CD

CIRCUIT DESCRIPTION OF THE
INSTRUCTION EXECUTION LOGIC/B (IXL/B)
(410401)

Sheet 2

REVISIONS

ISSUE	DATE	AUTH. NO.
1	3-18-75	23863R

SHEET NUMBER

21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
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SHEET ISSUE NUMBER

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.
		<i>DM</i>

ENG. SA/GH

DATE 2/28/75

R&D FILE NO.
6-167.172AA

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DRN.

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SECTION I - USER INFORMATION

1. General Description

1.1 The Instruction Execution Logic (IXL) requires two card assemblies - the IXL/A and IXL/B inserted into card positions 1 and 2 of the Logic Module. The Instruction Execution Logic provides the logic required to execute a sequence of instructions for the 40C400 Controller.

1.2 The IXL is divided into Data Path Logic and Sequence and Control Logic. The Data Path Logic receives data from the Telebus, processes the data and returns the data to the Telebus. The IXL/A card comprises the logic for the data path. The Sequence and Control Logic contained on the IXL/B card decodes the instruction stream so as to sequence the data path operations. The Instruction Set is composed of Instructions, Figures 1 through 7, and the Operand Addressing modes, Figures 8, 9 and 10. Table 1 lists the abbreviations used to describe the Instruction Set. The Instructions are divided into the following categories:

1.2.1 Double Operand Instructions - The Double Operand Instructions, shown in Figure 1, require both Source and Destination Addressing, shown in Figures 8 and 9.

1.2.2 Single Operand Instructions - The Single Operand Instruction, shown in Figure 2, require only Destination Addressing.

1.2.3 Branch Instructions - Figure 3 lists the Branch Instructions.

1.2.4 Jump and Return Instructions - Figure 4 lists both Jump and Return Instructions.

1.2.5 Data Block Instructions (Control Instruction Group) - Figure 5 lists the Data Block Instructions.

1.2.6 Diagnostic Instructions (Control Instruction Group) - The Diagnostic Instructions are listed in Figure 6.

1.2.7 Status Register Instructions (Control Instruction Group) - Figure 7 lists the instructions that can set or clear the Status Register.

1.3 The IXL/B card executes an instruction by first obtaining the instruction from the Telebus via the IXL/A card. The instruction is stored and decoded into a series of steps called microinstructions. In turn the microinstructions are decoded into control signals by a microprogram stored in an array of Read Only Memories (ROM). The series of microsteps, each approximately 1 microsecond in time, sequences the data through the data path to perform the instruction. When an instruction is completed, the next instruction is fetched.

1.4 The IXL/B also contains logic to command Telebus operations and logic to generate timing pulses to synchronize the operation of the Controller.

2. Features

2.1 The IXL/B card contains the capability to implement a Self-Test feature. This feature is provided by four LEDs and a momentary switch called the Self-Test switch installed on the upper edge of the card. Named Diagnostic LEDs, these LEDs are used to indicate the successful completion of the Self-Test routine, or to indicate the card position code of a card which has failed the Self-Test. Depressing the Self-Test Switch initiates a self-test microinstruction sequence within the IXL. If the IXL functions properly all four Diagnostic LEDs are energized. Releasing the Self-Test Switch continues the testing of the Controller by means of the Self-Test routine contained in the System Memory area.

2.2 In addition to the conventional Instructions, the IXL/B microprogram permits special instructions to be easily incorporated which enhance the performance of 40C400 Controller. These include instructions which speed up Display functions; Rapid Block Transfer (RBT), Store (STO), Search (SRH).

3. Supporting Information

3.1 Refer to 4401SD for schematics of the IXL/B card.

3.2 Refer to 4400CD and 4400SD for a description and the schematics of the IXL/A card.

TABLE 1

LEGEND FOR INSTRUCTION SET DESCRIPTION

LEGEND FOR SYMBOLS USED

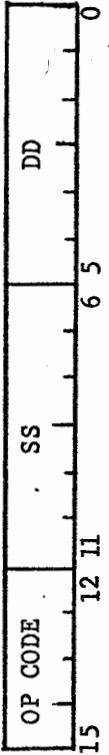
- = 0 for word/1 for Byte
- SS = Source Field (6 bits)
- DD = Destination Field (6 bits)
- JJ = Jump Address Field (6 bits)
- R = General Register 0 to 7 (3 bits)
- XXX = Offset, +127 to -128 (8 bits)
- YY = Parameter or selected status bits (4 bits)
- I = Index Word
- A = Valid Address
- N = Program Variable
- S = Contents of Source
- d = Contents of Destination
- PC = Contents of Program Counter
- SR = Contents of Status Register
- TR = Contents of Trap Register
- IR = Contents of Interrupt Register
- j = Jump Address
- n = Number of words in the data block operation

CONDITION CODE SYMBOLS USED

- * = Conditionally Set/Cleared
- = Unaffected
- 0 = Cleared
- 1 = Set

EXECUTION TIMES

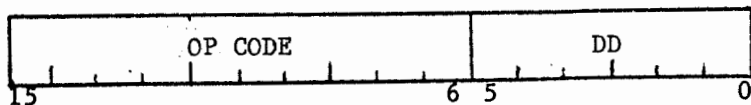
All times are in usec. Add 1.12 usec to source or destination operand addressing when accessing an I/O Device.



MNEMONIC	OCTAL CODE	INSTRUCTION	OPERATION	N Z C	EXECUTION TIME
MOV (B)	■ 1SSDD	MOVE	d ← s	* * 0	7.84
CMP (B)	■ 2SSDD	COMPARE	d - s	* * *	6.72
BIT (B)	■ 3SSDD	BIT TEST (AND)	d ∧ s	* * 0	6.72
BIC (B)	■ 4SSDD	BIT CLEAR	d ← d ∧ (¬s)	* * 0	7.84
BIS (B)	■ 5SSDD	BIT SET	d ← d ∨ s	* * 0	7.84
XOR (B)	■ 6SSDD	EXCLUSIVE OR	d ← d ⊕ s	* * 0	7.84
ADD	07SSDD	ADD	d ← d + s	* * *	7.84
SUB	17SSDD	SUBTRACT	d ← d - s	* * *	7.84

DOUBLE OPERAND INSTRUCTIONS

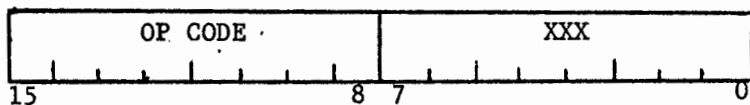
FIGURE 1



MNEMONIC	OCTAL CODE	INSTRUCTION	OPERATION	N Z C	EXECUTION TIME
CLR(B)	002DD	CLEAR	$d \leftarrow 0$	0 1 0	5.60
COM(B)	003DD	ONE'S COMPLEMENT	$d \leftarrow \bar{d}$	* * 0	5.60
INC(B)	012DD	INCREMENT	$d \leftarrow d + 1$	* * 0	5.60
DEC(B)	013DD	DECREMENT	$d \leftarrow d - 1$	* * 0	5.60
TST(B)	022DD	TEST	d	* * 0	4.48
ASL(B)	023DD	ARITHMETIC SHIFT LEFT	$d \leftarrow 2d$	* * *	5.60
ASR(B)	032DD	ARITHMETIC SHIFT RIGHT	$d \leftarrow d/2$	* * *	5.60
ROL(B)	033DD	ROTATE LEFT	$d \leftarrow 2d + c$	* * *	5.60
ROR(B)	042DD	ROTATE RIGHT		* * *	5.60
EXB	0043DD	EXCHANGE BYTES		* * 0	5.60
TSR	0052DD	TRANSFER STATUS REGISTER	$d \leftarrow SR$	- - -	5.60
TTR	0053DD	TRANSFER TRAP REGISTER	$d \leftarrow TR$	- - -	6.72

SINGLE OPERAND INSTRUCTIONS
FIGURE 2

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MNEMONIC	OCTAL CODE	INSTRUCTION	CONDITION
NOP	000400+XXX	No Operation	
BR	001400+XXX	Branch Unconditionally	Always
BNE	002400+XXX	BR If Not Equal	$\neq 0$ $Z = 0$
BEQ	003400+XXX	BR If Equal	$= 0$ $Z = 1$
BGE	004400+XXX	BR If Greater Than or Equal	≥ 0 $N = 0$
BLT	005400+XXX	BR If Less Than	< 0 $N = 1$
BGT	006400+XXX	BR If Greater Than	> 0 $NvZ = 0$
BLE	007400+XXX	BR If Less Than or Equal	≤ 0 $NvZ = 1$
BPL	100400+XXX	BR If Plus	$+$ $N = 0$
BMI	101400+XXX	BR If Minus	$-$ $N = 1$
BHI	102400+XXX	BR If Higher	$>$ $CvZ = 0$
BLS	103400+XXX	BR If Lower Than or Same	$\leq$ $CvZ = 1$
UNUSED	104400+XXX	-	
UNUSED	105400+XXX	-	
BCC(BHS)	106400+XXX	BR If Carry Clear	$\neq$ $C = 0$
BCS(BLO)	107400+XXX	BR If Carry Set	$=$ $C = 1$

If the branch condition is not satisfied, execution time is 2.24 usec.

If the branch condition is satisfied, branch to location. Execution time is 3.36 usec. $PC \leftarrow \text{Address of branch instruction} + 2 + (2 \cdot \text{offset})$.

BRANCH INSTRUCTIONS
FIGURE 3

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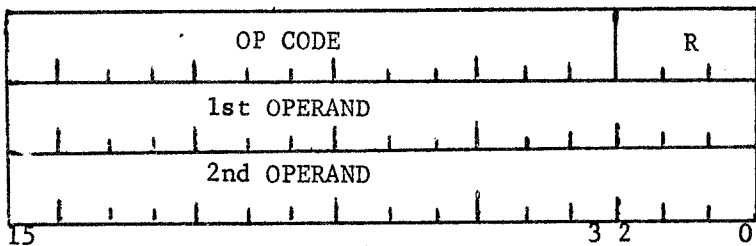


MNEMONIC	OCTAL CODE	INSTRUCTION	OPERATION	EXECUTION TIME
JMP	0072JJ	JUMP	$PC \leftarrow j$	5.60
JSR	0073JJ	JUMP TO SUBROUTINE	$SP \leftarrow SP - 2$ $(SP) \leftarrow PC$ $PC \leftarrow j$	10.08



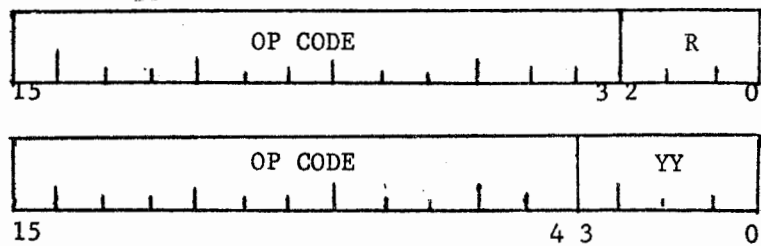
MNEMONIC	OCTAL CODE	INSTRUCTION	OPERATION	EXECUTION TIME
RTS	007267	RETURN FROM SUBROUTINE	$PC \leftarrow (SP)$ $SP \leftarrow SP + 2$	5.60
RTI	001140	RETURN FROM INTERRUPT	$SR \leftarrow (SP)$ $SP \leftarrow SP + 2$ $PC \leftarrow (SP)$ $SP \leftarrow SP + 2$	6.72
RFT	000120	RETURN FROM TRAP	$PC \leftarrow TR$	4.48

JUMP AND RETURN INSTRUCTIONS
FIGURE 4



MNEMONIC	OCTAL CODE	INSTRUCTION	OPERATION	EXECUTION TIME
RBT	001000	RAPID BLOCK TRANSFER	Moves a block of data from RAM to the Telebus. The first Operand defines block length. The second Operand defines the block address.	$17.92 + 1.12 \cdot n$
SRH	00202R	SEARCH	Search a block of data. $R0$ contains block addr. Rn defines block length. First Operand defines bits tested. Second Operand defines bit sense	$11.20 + 3.36n$
STR	00402R	STORE	Modifies a block of data. $R0$ contains block addr. Rn defines block length. First Operand defines bits cleared. Second Operand defines bit set.	$8.96 + 5.60n$

DATA BLOCK INSTRUCTIONS
FIGURE 5

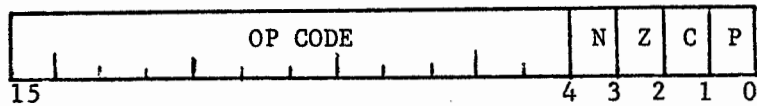


MNEMONIC	OCTAL CODE	INSTRUCTION
SWT	000000+YY	Software Trap
RTT	000060	Return from Trap and Trap
RTC	000160	Return from Trap, Trap and Clear T
LDT	00216R	Load Trap Register
RIV	00502R	Move Interrupt Vector Register to a General Register
-	00504R	Pause (Contents of R decremented until zero each 1.12 usec) (If contents of R is zero, 2 x 10 ¹⁶ cycles required)
-	005060	Issue Grant and Load IR with the Interrupt Vector
DLA	002000+YY	LED 0
DLB	003000+YY	LED 1
DLC	004000+YY	LED 2
DLD	005000+YY	LED 3

(Led on for period of cycles necessary to decrement 2YY to zero. If YY is zero, 2 x 10¹⁶ cycles required)

DIAGNOSTIC INSTRUCTIONS
FIGURE 6

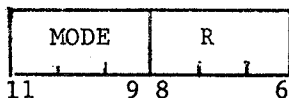
4401CD
Sheet 13
Issue 1



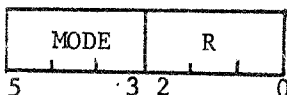
MNEMONIC	OCTAL CODE	INSTRUCTION	EXECUTION TIME
ZER N, Z, C, P	000100+ZZ	Clear the Selected Status Register Bits	4.48
SET N, Z, C, P	000140+ZZ	Set the Selected Status Register Bits	4.48

STATUS REGISTER INSTRUCTIONS
FIGURE 7

4401CD
Sheet 14
Issue 1



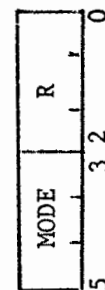
MODE	NAME	SYMBOLIC	DESCRIPTION	EXECUTION TIME
0	REGISTER	R	The Operand is contained in General Register R	0.00
1	REGISTER AUTO-DECREMENT	-(R)	Decrement R. The Address of the Operand is contained in R.	1.12
2	ABSOLUTE	A	The Address of the Operand is contained in the second word of the Instruction	1.12
3	IMMEDIATE	#N	The Operand is contained in the second word of the Instruction	0.00
4	REGISTER DEFERRED	(R)	The Address of the Operand is contained in General Register R.	0.00
5	REGISTER AUTO-INCREMENT	(R)+	The Address of the Operand is in R. After the Operand is accessed, R is incremented	0.00
6	RELATIVE	\$A	The Address of the Operand is the sum of the second word of the Instruction and PC	3.36
7	INDEXED	+I(R)	The Address of the Operand is the sum of the second word of Instruction and R.	3.36

SOURCE OPERAND ADDRESSING
FIGURE 8

MODE	NAME	SYMBOLIC	DESCRIPTION	EXEC. TIME
0	REGISTER	R	The Operand is contained in R.	0.00
1	REGISTER AUTO-DECREMENT	-(R)	Decrement R. The Address of the Operand is in R.	2.24
2	ABSOLUTE	A	The Address of the Operand is contained in the last word of the Instruction	2.24
3	ABSOLUTE DEFERRED	@A	The Address of the Address of the Operand is contained in the last word of the Instruction	3.36
4	REGISTER DEFERRED	(R)	The Address of the Operand is in R.	1.12
5	REGISTER AUTO-INCREMENT	(R)+	The Address of the Operand is in R. After the Operand is accessed, increment R.	1.12
6	RELATIVE	\$A	The Address of the Operand is the sum of the last word of the Instruction and the PC	4.48
7	INDEXED	+I(R)	The Address of the Operand is the sum of the second word of the Instruction and R	4.48

DESTINATION OPERAND ADDRESSING

FIGURE 9



MODE	NAME	SYMBOLIC	DESCRIPTION	EXEC. TIME
0	REGISTER DEFERRED	(R)	The Jump Address is contained in R.	0.00
1	REGISTER AUTO-DECREMENT DEFERRED	@-(R)	The contents of R are decremented. The Address of the location which contains the Jump Address is in R.	1.12
2	RELATIVE	\$A	The Jump Address is the sum of the second word of the instruction and the PC.	1.12
3	INDEXED DEFERRED	@+I(R)	The sum of the second word of the instruction and R is the address of the location containing the jump address.	3.36
4	ABSOLUTE	A	The Jump Address is the second word of the instruction.	0.00
5	ABSOLUTE DEFERRED	@A	The second word of the instruction is the address of the location containing the Jump Address.	1.12
6	REGISTER AUTO-INCREMENT DEFERRED	@(R)+	The contents of R is the address of the location containing the Jump Address. The register is post incremented.	0.00
7	TEST			

JUMP ADDRESSING

FIGURE 10

SECTION II - DETAILED DESCRIPTION

1. General Introduction

1.1 Purpose of Circuit

1.1.1 The CC4401 IXL/B Circuit Card Assembly contains the logic required to accept instructions and other external inputs and generally a proper sequence of control signals in response to each such instruction or external input. The control sequences, in turn, govern the detailed activity of the Data Path Card (IXL/A) and Telebus to execute the function specified by the instruction or specific external input.

1.2 Microprogram

1.2.1 The Instruction execution logic for any Programmable Controller, like the 40C400, usually consists of two subunits. One of these subunits, the Data Path Logic is required to perform storage, and arithmetic and logical manipulation of all operands and addresses as required by the instruction set of the controller. The other subunit is the Control Logic which interprets the instruction and issues a series of commands to the various logic elements in the data path (such as the registers, arithmetic logic or data switches or bus) in response to each instruction in the operating program. The 40C400 IXL/B control unit uses a technique called "microprogramming" to implement the proper sequencing of these controls. All control commands to the Data Path and Telebus originating from the Control Unit during a given IXL clock period constitute a control word or "micro-instruction". A sequence or collection of microinstructions is called a "microprogram" or microsubroutine and constitutes the actual step by step control of operations within the IXL.

1.3 Control Word

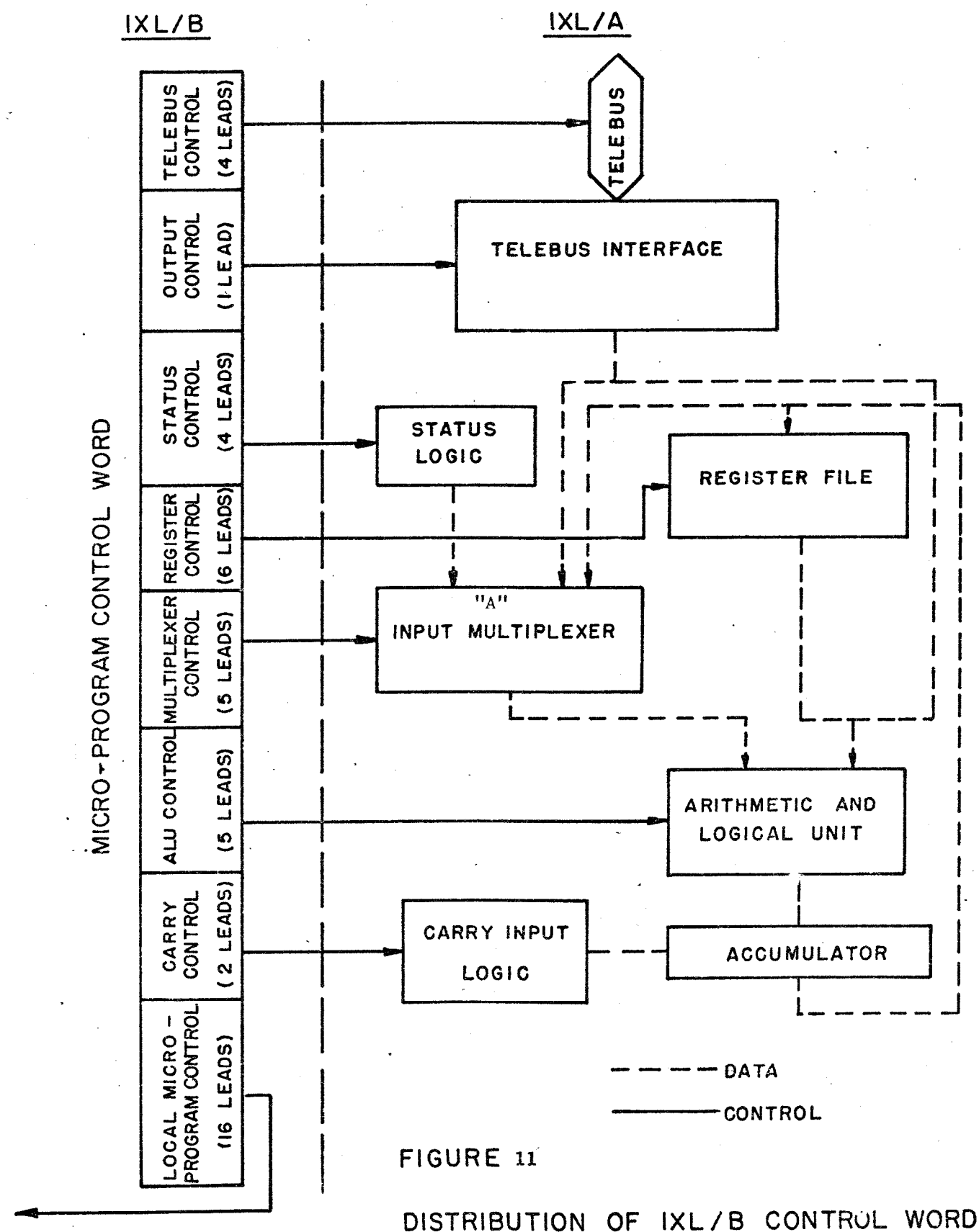
1.3.1 The microinstruction control word for the 40C400 is divided into a number of control fields each designed to control a specific logic element of the IXL as shown in Figure 11. A detailed account of these fields and their coding will be presented in subsequent sections.

1.4 Control Storage

1.4.1 The entire microprogram of the 40C400 consists of 256 control words stored in ROM arranged in groups or "microroutines". Each routine has a name and performs a specific function in the course of instruction execution as follows:

1.4.2 The FETCH microroutine accesses the next macro instruction and services the overhead functions for interrupts, traps or self tests.

1.4.3 The SOURCE microroutine accesses the first operand for all double operand instruction. The operand can be addressed in any one of 8 different addressing modes. See Figure 9.



1.4.4 The DESTINATION microroutine accesses the second operand for all double operand instructions or the only operand for single operand instructions. It also accesses the jump address for all jump instructions. Again, the operand can be accessed in any one of 8 different addressing modes. See Figure 10.

1.4.5 The SOURCE II and DST II microroutines are an extension of the SRC and DST routine which sign-extend and swap byte operands for subsequent manipulation by the ALU.

1.4.6 The EXECUTE microroutine controls the actual arithmetic or logical operations performed on the previously accessed operands.

1.4.7 The CONTROL microroutines perform the data manipulations required to execute the Control Type instructions such as RBT, SRCH and STORE.

1.4.8 The BRANCH microroutine performs the arithmetic calculations required to perform the branching instructions.

1.5 Major State Transition

1.5.1 For correct execution of a macro-instruction, the Control Unit must select one or more microroutines to be executed in sequence. The proper sequencing of these microroutines for any given macro-instruction is shown in Figure 12 in terms of a major state transition diagram. When the machine is executing a particular microroutine (such as FETCH) it is said to be in a major state. At any given time, the selection of the next major state, or microroutine depends on the present major state and the type of macro instruction being executed. All such conditions and their corresponding micro-program state transitions are shown in Figure 12.

1.6 Microprogram Next State Address Encoding

1.6.1 Since each major state, or microroutine of the machine corresponds to the execution of a distinct block of control words in the 256 word micro-program, a starting address for that particular section of ROM must be generated for each transition to its corresponding major state. It should be noted, however, that some major state microroutines divide into a number of smaller sub-blocks. Each sub-block in the routine performs a different variation of the required basic microroutine function. For example, the SOURCE and DESTINATION routines are actually divided into 8 sub-groups each; each performing the accessing of the SOURCE or DESTINATION operand in one of the 8 possible addressing modes. Thus, in addition to selecting the correct microroutine, the starting address generated upon major state transition must select the proper segment within the routine.

1.6.2 An overview of the 256 word microprogram layout is shown in Figure 13. For a detailed account of the step by step microprogram operation the reader is referred to a complete microprogram listing in a later section.

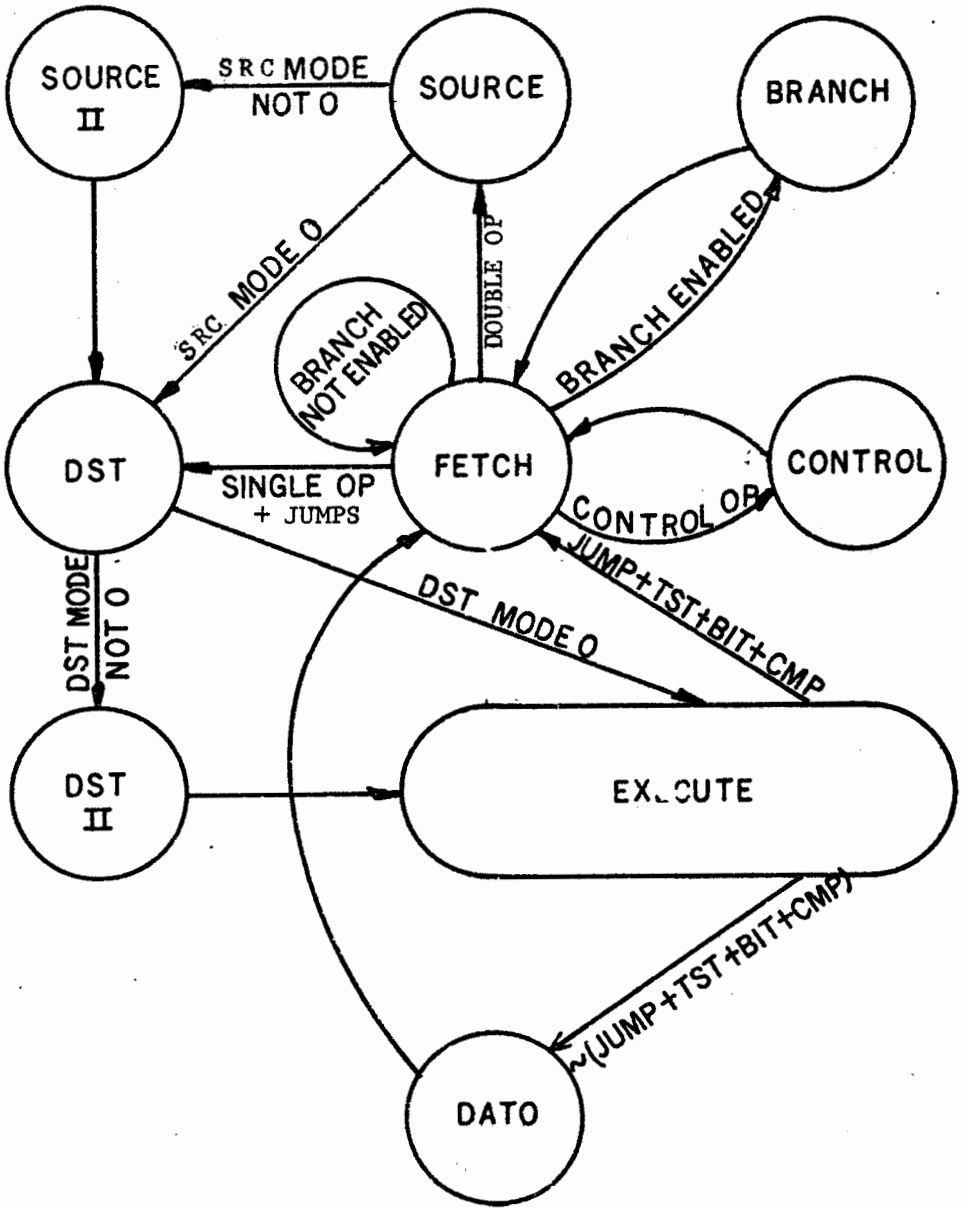


FIGURE 12 MAJOR STATE TRANSITION DIAGRAM

OCTAL ADDRESS	0-37	40-77	100-137	140-177	200-237	240-277	300-337	340-377
	FETCH	SOURCE	DESTINATION	DESTINATION BRANCH (142-143)	CONTROL		CONTROL	EXECUTE (340-357)
							SRC II (310-317)	DATO (360-367)
							CONTROL	EXECUTE (370-377)
							DST II (330-337)	

FIGURE 13 256 WORD MICRO-PROGRAM LAYOUT

2. Voltage and Logic Standards

2.1 The 410401 Card Assembly requires +5 Volts and +5 Volts Standby from the power supply. The voltage drop of the power busses on the 410401 Card is held to less than 2%. The power supply system should provide +5 Volts and +5 Volts Standby with sufficient tolerance to include the 2% due to card voltage drop and still provide +5 Volts $\pm$ 10% at the supply leads of all integrated circuit packages.

2.2 The following convention is used in the circuit description to give a unique designation to each circuit in an integrated circuit package.

MLB8 -- (4)

ML refers to micrologic

B8 refers to the package at board location B8

(4) refers to the pin number of the output of the circuit.

2.3 The terms "HIGH" and "LOW" are used in this description to indicate logic voltage levels; where "HIGH" represents any voltage between 2.4 and 5.5 volts and "LOW" represents any voltage between 0.0 and 0.4 volts.

2.4 Signal leads are labeled with a title description of its function. When they are superscribed with a bag (e.g., INTR) it indicates that the signal is in the LOW state when the state described by the signal is present; otherwise it is in the HIGH state.

3. Block Diagram

3.1 (Refer to 4401SD Sheet 2)

The schematic documentation of the 410401 Circuit Card Assembly (4401SD) is broken up into a number of Functional Schematics (FS1-FS8). The operation of each functional block will be described in this section. The block diagram (4401SD Sheet 2) shows the logical relationship of the functional blocks to each other.

4. Circuit Card Operation

4.1 FS-1 - INSTRUCTION REGISTER (Refer to 4401SD Sheet 3). All macro-instructions which are executed by the IXL are first brought into and stored in a 16 bit register called the Instruction Register (MLC11, 12, 13). The instructions originate from memory and are transmitted via the Telebus and received by bus transceivers located on the IXL/A circuit card. From there, they are transmitted on the back (B) connector to the instruction register on the IXL/B card. The proper signal for strobing of the instruction is generated by gate MLB14-(12). Strobing of the instruction occurs when the FB1 and FB2 leads, part of the microprogram control word, are LOW and the ACC CLOCK lead, originating in the Timing Logic (FS-8) goes LOW.

4.2 FS-2 - INSTRUCTION DECODE AND MAJOR STATE CONTROL LOGIC (Refer to 4401SD Sheets 3 and 4).

4.2.1 The instruction decode ROM (MLB11) and outputs 2 and 3 of the branch ROM (MLC9) are used to decode certain attributes of the instruction currently being executed. These attributes are required by the address encoding logic and affect the microroutine starting address as follows:

4.2.1.1 BYTE - The instruction is a byte operation. This attribute affects starting address encoding in the SOURCE, SOURCE II, DESTINATION, DST II and DATO routines.

4.2.1.2 SUBTRACT - The instruction is a subtract instruction. This condition affects address encoding in the DOUBLE OP routine.

4.2.1.3 BYTE A (MOVBA DMO) - The instruction is a byte operation; but not a MOV destination mode 0. This attribute is needed to control the starting address in the DATO routine.

4.2.1.4 DMO - The instruction has a destination mode of 0. This condition affects the address encoding in the DATO routine.

4.2.1.5 JUMP - The instruction is either a JMP or JSR instruction. This attribute affects address encoding in the DESTINATION state.

4.2.1.6 ROR - The instruction is a ROR. Starting address of the SRC II and DST II routine is affected.

The Boolean equation for decoding these attributes is also shown on FS2. The detailed relationship between the above attributes and the micro-routine starting addresses is described in the explanation of the M.P. address encoding logic (FS-3).

4.2.2 The Branch ROM (MLB11) in addition to decoding instruction attributes, compares the instruction bits which identify the branch type (IR9-IR11 and IR15) with the condition codes C, Z and N originating in the Status Register on IXL/A. Whenever the value of the condition codes satisfies the condition imposed by the branch type, a HIGH level is generated on the BR ENABLE output MLC9-(12). This output, in turn, is fed to the next state ROM (MLC10) and affects a state transition to the BRANCH routine if the instruction is a branch type.

4.2.3 The Next State ROM (MLC10) receives two groups of information. The first group (PS0, PS1 and PS2) contains a code which conveys the present major state of the control unit. This code is part of the microprogram control word and is generated by the micro-control ROM ML11 (10-12) on FS4 as a direct result of the microprogram address. The second group (BR ENABLE, IR7, IR8, DBLOP and ROR) conveys information necessary to decode the type of instruction currently being executed. The Next State ROM combines this information and generates a coded output on MLC10 (9-12) which signifies the next microroutine to be executed. This next state code (NS0-NS3) is sent to the microprogram address encoding logic (FS3) and selects the proper address encoding for each

4.2.3 Continued

particular microroutine. 4401SD Sheet 5, Table 1, shows a detailed major state transition table, which describes, in symbolic and binary form, the coding of the MLC10 Next State ROM. The first part of the table indicates a micro-program address field and the corresponding microroutine or major state, located in the field. The present major state code (PS0-PS2), generated from the address field by the control ROM ML11, is shown alongside the name of the present state. For each present state, the table shows one or more transitions to a next state, whose name and code (NS0-NS3) are shown at the right. Where there is more than one possible transition, as in FETCH, the particular next state depends on the instruction type currently being executed. The information necessary to decode instruction type is listed along the name of the type. Note that in some cases, more than one present major state is assigned to a particular coding of PS0-PS2, for example in BRANCH, CONTROL and DATO. This is done to minimize the code since, in each such instance, the next state is the same. Also, the next state code is assigned in such a manner as to simplify the address encoding logic shown later. It can be seen that the transition table is simply a more detailed version of the transition diagram of Figure 12.

4.2.4 The gate MLB14-(6) decodes the DBLOP attribute which is required by the next state ROM and by the branch ROM to decode the ROR and JMP attributes.

4.3 FS-3 Micro-Program Next State Address Encoding Logic (Refer to 4401SD Sheet 4)

4.3.1 The next state code (NS0-NS3) generated by the MLC10 ROM controls the selection of microroutine starting addresses as follows. Each bit of the starting address for a given microroutine forms an input to a 1 of 8 multiplexer. Since 8 bits of address must be generated to produce an entire next microroutine address, 8 channels of multiplexing are required to generate the whole address set. For each particular next state code, a set of 8 inputs is chosen to be gated through to the next state microprogram address bus (NS ADDRS0-NS ADDRS7). Each microroutine starting address, generated in this manner, is not a fixed value but is dependent on certain attributes from the instruction itself. The binary value of these attributes cause a modification of the entry point in a given microroutine. For example, the starting address for the SOURCE routine is selected by NS code = 5 (octal) which gates the "D5" inputs of multiplexers MLB6 through MLB9 and MLC6-C7 to the "NS ADDRS" bus. A number of attributes modify the SOURCE routine starting address as follows:

- a) BYTE on address bit 1 (NS ADDRS1)
- b) IR9 on address bit 2 (NS ADDRS2)
- c) IR10 on address bit 3 (NS ADDRS3)
- d) IR11 on address bit 4 (NS ADDRS4)

Thus there are really 16 different sub-block starting addresses, or encoding combinations, for this particular routine. A pair of different microprogram sub-blocks, in this case, controls the execution of one of the eight source operand addressing modes, one sub-block of each pair in the word mode and one in the byte mode, as seen in the detailed microprogram listing. Note that the attributes IR9-IR11 correspond directly with that part of the instruction word which specifies the source addressing mode.

4.3.2 Table 2 of 4401SD Sheet 5 shows the address encoding selection for each of the nine major states or microroutines of the Control Unit. The SRC II and DST II state encoding has been combined to form a single input into the 1 of 8 address selector multiplexers. The starting addresses for these two microroutines differ only in bit position 4 (SRC II bit address bit 4 is LOW, and DST II address bit 4 is HIGH). Since the Present State code lead PS1 is LOW in the SOURCE state and HIGH in the DESTINATION state, this lead is used as an attribute in address bit position 4. It should be noted that the encoding for address bits 6 and 7 (NS ADDRS6 and NS ADDRS7) is done by dual 4-1 multiplexer MLC8 since the upper address bits have the same value for more than 1 microroutine. For example the FETCH and SOURCE routines both have address bits 6 and 7 LOW; the DESTINATION and BRANCH have address bit 6 HIGH and address bit 7 LOW, etc. The microroutines are subdivided into four such groups, and thus it only becomes necessary to select the group, instead of the exact routine. The next state code bits NS2 and NS3 are assigned so that they select such a group of these routines.

4.3.3 Multiplexer MLB10 is used to select 1 of 2 sets of attributes and combines them into 1 set for use by the EXECUTE microroutine. Since the "routine address determining" bits for a Double-Operand Instruction are IR12, IR13 and IR14 and for a Single Operand instruction are IR6 and IR9-11, MLB10 selects between the two sets. The resulting outputs are called EXEC0 through EXEC3 and are gated to the microprogram address bits 0, 1, 2 and 4, upon entry into the EXECUTE microroutine. The Subtract instruction disables the outputs and causes LOWs to be applied to the particular microroutine address positions. Both the "DBL OP" and "SUBTRACT" leads originate in the Instruction decode logic (FS-2).

4.3.4 Gates MLB15 and MLB16 generate the attributes required for handling interrupts, traps and self tests in the FETCH state, since each of these conditions require the execution of a different FETCH microprogram sub-block. For example the "INTR" condition, along with LOWs in the "T" and "P" status register bits, will generate a HIGH on microprogram address bit 2, if there is no "TRAP" or self TEST pending; causing an entry into the FETCH microroutine at octal address 4. Normal entry into FETCH is made at octal address 2 since the absence of all external conditions causes a HIGH level on the MLB15-(13) gate, (TEST TRAP INTR T P), which is gated, via the MLB7 multiplexer, into microprogram address bit 1. Similarly the self TEST and TRAP conditions cause an entry at octal address 20 and 10 respectively, due to HIGH level generated on the TEST or TRAP*TEST leads which are gated into levels 4 and 3 of the microprogram address prior to the execution of the FETCH microroutine.

4.3.5 The exact address generated for each specific entry into a microroutine can be read from the Address Encoding Table of 4401SD Sheet 5. By imposing, upon each address bit, the attribute specified in the table, the total address is derived. If the specific attribute is a "H" or "L", the corresponding address bit is fixed at entry into that microroutine. If the attribute is an Instruction Register bit, such as IR9, the address is dependent upon the value of that bit when the microroutine is executed. If the attribute is a more complex boolean expression, it must be evaluated to establish the microroutine next state address.

4.4 FS-4 Micro-Program Addressing Logic and Micro-Storage Array No. 1

4.4.1 Microprogram Addressing Logic

4.4.1.1 Two 4 bit presettable counters, MLA6 and MLA7, make up an 8 bit micro-program address register. The outputs of this register drive the address lines of the entire 256 word ROM microprogram storage array. The lower 4 bits of the counter receives 2 sources of preset data via the MLA5 quad 2-1 multiplexer. One source comes from the next state address encoding logic on FS3, labeled NS ADDR0 through NS ADDR3, and the other source comes from the ROM microprogram control word and is labeled MPBR ADDR0 through MPBR ADDR3. The upper 4 bits of address can be preset with encoding logic outputs NS ADDR4 thru NS ADDR7.

4.4.1.2 Whenever transfer to a new microroutine is to be executed, the address register is preloaded with the routine starting address on the NSADDR leads generated by the address encoding logic. Within a given microroutine, however, sequential addresses are generated on the MPBR ADDR leads by the micro-ROM itself, and are loaded into the lower 4 bits of the micro-program address register one after another at each IXL cycle as the microroutine proceeds until a new next state starting address is required. This activity is controlled by the leads labeled SEQ0 and SEQ1, which are also part of the microprogram ROM outputs. Thus when SEQ0 and 1 are both HIGH, a load of 8 bits from the NS ADDR leads occurs because MLC17-(1) and MLC17-(4) are both LOW, and when SEQ0 is LOW and SEQ1 is HIGH a load of the lower 4 bits from the MPBR ADDR ROM outputs occurs because MLC17-(1) is LOW and MLC17-(4) is HIGH.

4.4.1.3 Conditional Loading - Whenever lead SEQ1 is LOW the MLA6 preset is conditioned by the CNT EN lead. This lead originates on the IXL/A card and indicates the success or failure of a microprogram level test. The test indicates that the result of the ALU operation currently being executed is either zero or non-zero. The SEQ0 lead is sent to the IXL/A card and selects a zero test when in a LOW state and a non-zero test when in a HIGH state. When the particular test fails, the IXL/A sends a LOW level on the CNT EN lead. This condition, together with SEQ1 lead being LOW, causes the address register to index (count) rather than preset to a next address. Using this technique the microprogram can do conditional branching within a microroutine. This feature is frequently employed within the microroutines for the SEARCH, STORE and other instructions in the CONTROL group. The address register is clocked every IXL cycle with the MP CLOCK lead which originates in the Timing Logic (FS-7). A HIGH condition on the PWR RESET lead going to MLA6 and MLA7 causes these registers to be reset to all LOWs. This condition will initiate micro-program execution at address 0, which corresponds to the power up microroutine. (See microprogram listing.)

4.4.2 Micro-Storage Array No. 1

4.4.2.1 The succession of microprogram addresses, from the address register MLA6-MLA7, feeds the ROM microprogram arrays No. 1 and 2 which, in turn, generate the 44 bit micro-control words required to control the IXL and TELEBUS. Micro-ROMs MLA9 thru MLA13 generate the following control fields:

4.4.2.1 Continued)

- a) Control ROM MLA9 generates the MPBR ADDRESS field. This 4 bit field specifies the low-order part of the next microprogram address location to be executed on the next IXL clock cycle.
- b) Control ROM MLA10 generates a 4 bit BUS CONTROL field. The leads MPC0-MPC2 specify the bus operation (e.g., load-address and read) to be executed during the upcoming TELEBUS cycle. The lead MPINTG specifies that the interrupt grant (INTG) lead of the TELEBUS is to be activated.
- c) Control ROM MLA10 -(10-12) generate the 3 bit present state code (PS0-PS2) which converts the microprogram address fields, corresponding to a specific microroutine, into the codes specified by the NEXT State Table (4401SD Sheet 5). Control ROM MLA10-(9) generates a single "OUT ENABLE" which controls the IXL/A TELEBUS output gating.
- d) Control ROM MLA12 generates a 4 bit STATUS CONTROL code field. These leads control the loading, setting or clearing of the N, C, Z, P and T status bits residing in a register on the IXL/A card.
- e) Control ROM MLA13-(9, 10) generate a 2 bit ALU carry input control code. This code specifies the value of the ALU input carry and the value of the sign extension during the upcoming IXL cycle. Control ROM MLA13-(11,12) generates the two sequence control leads (SEQ0 and SEQ1) required to control the cycle by cycle activity of the microprogram address register, described in 4.4.1.

4.4.2.2 Detailed listing of the above control codes and their specific functions are found in the tables accompanying the 4401SD Sheet 6. An explanation of the functions controlling the IXL/A card can be found in the 4400CD.

4.5 FS-5 Micro-Program Storage Array No. 2 and General Purpose Register Addressing Logic.

4.5.1 M.P. Storage Array No. 2

4.5.1.1 This part of the microprogram storage consists of MLA3 and MLA14 through MLA18 and generates the following control fields:

- a) Control ROM MLA8 generates the 4 LED control leads LED0 through LED3. These leads, when programmed in a HIGH state, light their corresponding LED during the upcoming IXL cycle. The feature is used for the IXL self test operation and by program execution of the LED macro-instructions.
- b) Control ROM MLA14-(9-11) generates a 3 bit code (FB0-FB2) which controls the loading of the macro-instruction (see 4.1), clearing and setting of the TRAP condition and sampling or clearing of the Odd byte condition as described in detail in Section 4.6.
- c) Control ROM MLA14(12) and MLA15 provide the ALU function code (MPS0-MPS3 and M) to the IXL/A card. The function code specifies the logical or arithmetic operation to be performed by the ALU during the upcoming IXL

4.5.1.1 Continued

c) continued

cycle. Whenever the "M" lead is LOW, the operation is of an arithmetic nature, whereas when "M" is HIGH the operation is of a logical type.

d) Control ROM MLA16 and MLA17 (9-11) generate the IXL/A Register File Control field. The leads MP REG SEL0 through MP REG SEL4 select the specific register of the file to be accessed during the upcoming IXL cycle. The leads MP WUB and MP WLB specify that the upper or lower byte (or both), of the selected register are to be loaded on the upcoming cycle. These control leads are routed to the Register File addressing logic described in Section 4.5.2.

e) The Control ROMs MLA17-(12) and MLA18 generate a 5 bit IXL/B input multiplexer control code MUX SEL0 through MUX SEL4. This code selects a specific operand or value to be selected for presentation to the IXL/A ALU A operand bus during the upcoming IXL cycle. The choices of operands include the TELEBUS input, the Accumulator, and the Status Register. Additional multiplexed operand sources are the constant values +1 and -2, sign extended operands and byte exchanged operands from the above sources.

4.5.1.2 A detailed listing of the functions of the above control codes are to be found in the accompanying tables on 4401SD Sheet 8. An explanation of the functions controlling the IXL/A card can be found in the 4400CD.

4.5.2 Register File Addressing Logic - Register file addresses, sent to the IXL/A circuit card, originate from three sources in the IXL/B control logic.

Whenever a double operand instruction is being executed, instruction register bits IR6, IR7 and IR8 can specify the 1 of 8 general purpose registers to be used for the source operand or the source operand address. Whenever a double or single operand instruction or control instruction is being executed, instruction register bits IR0, IR1 and IR2 can specify 1 of 8 general purpose registers to be used for the destination operand or destination operand address.

During the course of execution of a microroutine, the microprogram, itself, may specify the implied use of any of the 8 general purpose registers in a given instruction, such as the use of Register 0 for the block starting address of a SEARCH or STORE instruction. Additionally, the microprogram may address any of the remaining 8 special purpose registers of the IXL/A register file. These registers are used to handle various overhead functions as follows:

- a) PC (register 8) used as a macro-instruction program counter.
- b) SRC (register 9) used to temporarily store the SOURCE operand until execution of arithmetic or logical operation.
- c) TEMP (register 10) used as a temporary register for storage of one of the mask operands during the execution of the SEARCH and STORE instruction.

4.5.2 Continued

- d) X (register 11) used as a temporary register for storage of intermediate results during the execution of the SEARCH and STORE instructions.
- e) IV (register 14) is used to store the last interrupt vector generated by a device on the TELEBUS. This feature is a diagnostic aid.
- f) TRAP (register 15) is used to save the value of the program counter when a TRAP condition is serviced. The PC is restored when a RETURN FROM TRAP instruction is executed.

The three-way register selection, described above, is done by the MLB12 and MLB13 4 into 1 multiplexers. The MP REG SEL4 lead, from the microprogram control word, selects "instruction selected" registers when in a LOW state and implied microprogram registers when in a HIGH state. When "instruction selected" registers are addressed the MP REG SEL0 lead, from the control word, selects the SOURCE instruction register field when in a LOW state and the DESTINATION instruction register field when in a HIGH state.

When implied microprogram registers are addressed, the leads MP REG SEL0 through MP REG SEL3 contain the binary address of the registers to be accessed during the upcoming IXL cycle. The 4 MLB12 and MLB13 outputs R0-R3 are routed via the back-bus (connector B) to the IXL/A circuit card.

4.6 FS-6 - Bus Control, Interrupt, Trap and Self Test Logic -(See 4401SD Sheet 9)

4.6.1 Bus Control Logic - TELEBUS transceiver MLB5 receives the 4 microprogram TELEBUS control leads MPC0-MPC2 and MP INTG, buffers these leads with "open collector" drivers and sends them out to the TELEBUS to control the BUS operations. Pins 7 and 9 are strapped to ground to permanently enable the BUS outputs.

The MLC14 decoder monitors the TELEBUS data/address lines and serves to decode two groups of TELEBUS addresses. The first group is address range 160000 to 161776 (octal) which defines the I/O device addresses falling into the "I/O A" selection group. The second range is 162000 to 163776 (octal) and defines the "I/O B" device selection group. Whenever an address falling into either of the two device ranges appears on the TELEBUS, the "I/O A" or "I/O B" leads are asserted LOW on MLC14-(9) and (7) respectively. These signals are inverted by the MLC15-(6) and (3) gates and converted to TELEBUS "open collector" signals by MLB4-(11) and MLC5-(15) respectively; from where they are routed along the BUS to the various I/O devices.

4.6.2 Interrupt and Trap Logic

The interrupt request, INTR, is received from the TELEBUS via the MLC5 (pin 6) bus transceiver. The received signal, R INTR, is transmitted to the MLB18 quad D flip-flop where it is synchronized with the positive edge of the ACC CLOCK signal from the timing logic. This is done to avoid critical races in the subsequent address encoding logic which has the synchronized INTR lead as an input to gate MLB16-(5).

4.6.2 Continued

The trap request, TRAP, is received from the TELEBUS via the MLC5 (Pin 1) bus transceiver. The received signal, R TRAP, is sent through the MLC17 NOR gate to 3 of the inputs of the MLB17 dual 1-4 selector. The feed back select code (FB0-FB2), originating from the microprogram control word ROM MLA14-(9-11), enables passage of the trap condition through the multiplexer when the FB1 and FB2 leads are not both HIGH. The output of the multiplexer is clocked into pin 12 of the MLB18 quad D flip-flop on the positive transition of the ACC CLOCK signal from the timing logic (FS-7). Once the D flip-flop is set from an external trap condition, the value of the flip-flop output PRE TRAP is looped back to provide the second input of the MLC17-(13) NOR gate. To terminate or reset such an external trap condition the microprogram FB0, FB1 and FB2 leads are all switched to a HIGH level, allowing a LOW level to be clocked into the flip-flop on the subsequent ACC CLOCK cycle. This is done by the first micro-step in the trap microroutine, since execution of this micro-step indicates that the above trap condition has been recognized and is being serviced by the micro-program.

The microprogram can also initiate a software trap, without an external trap condition. This is done by programming the FB0 and FB1 leads HIGH, and the FB2 lead LOW, which allows a HIGH level to be clocked into the MLB18-(10) D flip-flop. The "RETURN FROM TRAP WITH TRAP" (RTT or RTC) macro-instructions makes use of this feature since, at the end of its execution, the trap condition is reinitiated. This microprogram initiated trap condition is delayed by one IXL clock cycle since the PRE TRAP lead from MLB18-(10) is again synchronized with the positive edge of the IG CLOCK in the MLC16-(14) D flip-flop. This allows any software trap condition, generated at the end of RTT or RTC instructions to be delayed past the first step of the FETCH routine; allowing the next user instruction to be fully executed before the trap condition is again serviced. This mode of operation is used by the SODA debug system to emulate single instruction execution and the instruction trace techniques. The output of the MLC16-(14) flip-flop is called the TRAP lead and generates an input to the address encoding logic of FS-3, where it causes an entry into the TRAP sub-block of the FETCH routine at the end of the execution of the current instruction.

4.6.3 Odd Address Logic

Whenever the microprogram places byte operand addresses on the TELEBUS during the execution of a SOURCE or DESTINATION addressing mode, the low order bit (D/A0) of the address is tested for a "one" (LOW on TELEBUS). If this condition occurs, the byte operand subsequently delivered by the memory or I/O device exists on the upper 8 bits of the TELEBUS. The microprogram must swap the byte operand onto the lower 8 bits of the IXL/A data path to properly perform the required arithmetic or logical function. The controls for these operations is generated in ODD BYTE sub-block of the SRC II and DST II microroutines. Entry into these sub-blocks is controlled by the ODD BYTE lead from the MLB18-(14) D flip-flop which conditions the next state address encoding logic to the proper address of the sub-blocks.

4.6.3 Continued

The D/A0 bus lead is gated into the flip-flop via the MLB17 multiplexer whenever the FB0 lead is LOW and FB1 lead is HIGH. The odd byte condition is cleared from two places in the microprogram as follows:

- In the execution of the ODD BYTE sub-block of the SRC II routine. At this point the odd address condition generated during the accessing of the source operand has been recognized.
- In the execution of the instruction FETCH routine. At this point any odd address condition generated during the accessing of the destination operand has been satisfied. It should be noted that, for the destination operand address, the odd byte condition must be preserved until the DATO routine is executed. Since an odd destination address requires that the byte result must be re-swapped onto the upper 8 bits of the TELEBUS for depositing into the correct memory or I/O device location. This is done by the controls generated during the execution of the ODD BYTE sub-block of the DATO microroutine.

The clearing of the ODD BYTE condition in the MLB18-(14) flip-flop occurs when the FB0 lead is HIGH and FB1 lead is LOW. The state of the ODD BYTE condition is preserved whenever the FB0 and FB1 leads are both HIGH or both LOW.

4.6.4 Self Test Logic

An IXL self test is originated by depressing the switch SW1. The switch output level is synchronized with the positive going edge of the IG CLOCK lead to avoid races in the subsequent address encoding logic. The test flip-flop, MLC16-(2) delivers a LOW signal to the MLB16-(3) gate and a HIGH signal to the MLB15-(1) gate in the address encoding logic. When the self test condition is active, the microprogram TEST sub-block is selected upon entry into the FETCH microroutine (at the end of the present instruction). The TEST sub-block control sequence sets up and tests various conditions in the IXL/A data paths. Each time a test condition is successfully met, one of the LEDs on the IXL/B card is activated via the microprogram. If every condition of the self-test is met, all 4 LEDs will appear to be active during the depression of SW1; since the microprogram executes the self test repeatedly.

4.7 Micro-Program Symbolic Listing

Table 2 contains the complete symbolic listing of the 256 word microprogram. Each horizontal entry in the listing constitutes an entire microprogram control word. The first three columns contain the name of the microroutine, the names of the sub-blocks within the routine and the binary microprogram address. The remaining columns each contain the mnemonic symbols representing a given control operation performed by the microprogram control field specified in the heading. Table 2A is a legend containing an index of the symbols and their corresponding control operations.

TABLE 2A

LEGEND OF MICRO-PROGRAM LISTING MNEMONICS

ALU FUNCTION

The expressions listed in the table are the arithmetic or logical values appearing on the ALU output bus. The expressions are written in terms of the A and B operand busses of the ALU (see the table of ALU operations in the 4400CD).

"A" - MUX SELECT

- BUS - The contents of the TELEBUS are gated onto the A operand inputs of the ALU.
- BUS SX - The sign extended contents of the TELEBUS are gated onto the A operand bus of the ALU.
- BSWBSX - The contents of the TELEBUS are byte - swapped and sign extended and gated onto the A operand bus of the ALU.
- ACC - The contents of the Accumulator are gated onto the A operand bus of the ALU.
- ACC SX - The sign extended contents of the Accumulator are gated onto the A operand bus of the ALU.
- ACC SWB - The byte swapped contents of the Accumulator are gated onto the A operand bus of the ALU.
- ACC SR - The contents of the Accumulator are shifted right and gated onto the A operand bus of the ALU.
- STATUS - The contents of the Status Register are gated onto the A operand bus of the ALU.
- +1 - The constant 000001 (octal) is gated onto the A operand bus of the ALU.
- 2 - The constant 177776 (octal) is gated onto the A operand bus of the ALU.

REG. CONTROL

- "B" - REGISTER - The contents of the designated register is placed on the B operand bus of the ALU.
- WLB - A "1" symbol in the column indicates that the lower byte of the designated register is written into.

TABLE 2A
(Continued)

WHB - A "1" symbol in this column indicates that the high byte of the designated register is written into.

CARRY

CIN

- "0" - The carry input of the ALU is "0".
- "1" - The carry input of the ALU is "1".
- ACC15 - The carry input of the ALU is Accumulator bit 15.
- C - The carry input of the ALU is the Status Register "C" bit.

SX

- A7 - The value of the sign extension is derived from bit 7 of the multiplexer input bus.
- C - The value of the sign extension is derived from the Status Register "C" bit.

OUT EN

A "1" indicates that the contents of the "B" operand bus are gated out onto the TELEBUS.

BUS

CONTROL

- LAR - Sends the "load-address-and-read" bus command.
- LDA - Sends the "load-address" bus command.
- WWI - Sends the "write-word" bus command.
- WBI - Sends the "write-byte" bus command.
- RDI - Sends the "read and increment" bus command.
- RDV - Sends the "read from device" bus command.
- RDW - Sends the "read word" bus command.

G - A "1" indicates the "INTG" bus lead is active during this cycle.

LED - A binary combination used to activate the 4 LED's on the IXL/B card.

- Bit 0 activates LED0
- Bit 1 activates LED1
- Bit 2 activates LED2
- Bit 3 activates LED3

TABLE 2A
(Continued)

STATUS CNTRL

- CLR T - Clear the T bit of the Status Register.
SET T - Set the T bit of the Status Register.
XFR - Load the following bits of the Status Register:

"C" bit loaded with "0"
"N" bit loaded with ALU output bit 15
"Z" bit loaded if ALU output is 000000 (octal)

- ADD - Load the following bits of the Status Register:

"C" bit loaded with ALU carry output
"N" bit as in XFR
"Z" bit as in XFR

- SUB - Load the following bits of the Status Register:

"C" bit loaded with inverted ALU carry output
"N" bit as in XFR
"Z" bit as in XFR

- BUS - Load the entire status register from the output of the ALU.

SEQ CNTRL

- BR - Branch to the next control word. The next control word is located at the address designated by the concatenation of the 4 "BRANCH ADDRESS" bits and the upper 4 bits of the existing microprogram address.

- BR Z=1 - Branch to the next control word (as in BR) if the ALU output is 000000 (octal), otherwise index address counter for next address.

- BR Z=0 - Branch to the next control word (as in BR) if the ALU output is not 000000 (octal), otherwise index address counter for next address.

- DONE - Enter next major state microroutine address as defined by the address encoding logic.

F.B.

- CT - Clear the trap condition
ST - Sets the trap condition (software trap)
COB - Clear odd byte condition
OBE - Enables sampling of D/A0 lead to test for odd byte condition
LIR - Loads the macro-instruction register

TABLE 2B

MICRO-PROGRAM SYMBOLIC LISTING

MICRO ROUTINE	SUB CLOCK	BINARY ADDRESS	ALU FUNCTION	'A'-MUX SELECT	REG. CONTROL	CARRY	OUT EN	STATUS CNTRL	BUS CNTRL	LED	SEQ CNTRL	BRANCH ADDRESS	F.B.
FETCH	PUR UP	0000000	A	-2	SRC	0	0	CLRT	NAP	0000	BR	0001	CT
	FETCH	00001	A	+1	SRC	0	0	BUS	NAP	0000	BR	1011	NAP
		00010	A+B+1	+1	PC	1	1	NAP	LAR	0000	BR	0011	COB
		00011	A+A	BUS SX	SRC	0	0	NAP	NAP	0000	DONE	1111	LIR
		00100	A+B	-2	SP	0	0	NAP	NAP	0000	BR	0101	NAP
		00101	A+B	-2	SP	0	0	NAP	LDA	0000	BR	0110	NAP
		00110	A	STATUS	PC	0	0	NAP	WWT	0000	BR	0111	NAP
		00111	A	+1	SP	0	0	BUS	LDA	0000	BR	1101	NAP
		01000	B	BUS	PC	0	0	SET T	NAP	0000	BR	1001	CT
		01001	A	ACC	TRAP	0	0	NAP	NAP	0000	BR	1010	NAP
		01010	A+A	-2	SRC	0	0	NAP	NAP	0000	BR	1011	NAP
		01011	B	BUS	SRC	0	0	NAP	LAR	0000	BR	1100	NAP
		01100	A	BUS	PC	0	0	NAP	NAP	0000	BR	0010	NAP
		01101	B	BUS	PC	0	0	NAP	WWT	0000	BR	1110	NAP
		01110	A	BUS	IV	0	0	NAP	RDV	0000	BR	1111	NAP
		01111	B	BUS	IV	0	0	NAP	LAR	0000	BR	1100	NAP
		10000	A+1	-2	R3	1	0	BUS	NAP	0001	BR Z=1	0000	CT
		10001	A+1	ACC SX	R0	1	0	ADD	NAP	0001	BR Z=1	0011	NAP
		10010	A+B+1	BUS	PC	0	0	NAP	NAP	0001	BR	0100	LIR
		10011	A+A+1	+1	PC	0	0	NAP	NAP	0001	BR	0010	NAP
		10100	A+A	ACC SX	RD	0	0	CLRT	NAP	0001	BR	0101	NAP
		10101	A-B	ACC SWB	RS	0	0	NAP	NAP	0001	BR	0110	NAP
		10110	A+B	STATUS	R3	0	0	NAP	NAP	0001	BR	0111	NAP
		10111	A+B	+1	RD	0	0	XFR	NAP	0001	BR Z=1	0000	CT
		11000	A+B	ACC SX	R3	0	0	NAP	NAP	0010	BR	1001	NAP
		11001	A+B+1	ACC	RD	0	0	NAP	NAP	0010	BR Z=0	1011	NAP
		11010	A+B+1	ACC	R0	0	0	NAP	NAP	0010	BR	1100	NAP
		11011	A+B+1	BUS SX	R3	0	0	NAP	NAP	0010	BR	1010	LIR
		11100	A	ACC	R4	0	0	NAP	NAP	0010	BR Z=0	1100	NAP
		11101	A+B	ACC SX	RD	0	0	NAP	NAP	0010	BR	1110	NAP
		11110	A+B	ACC SX	RS	0	0	NAP	NAP	0010	BR	1111	NAP
		11111	B	BUS	R0	0	0	NAP	NAP	0010	DONE	1111	NAP

MICRO-PROGRAM SYMBOLIC LISTING

MICRO ROUTINE	SUB BLOCK	BINARY ADDRESS	ALU FUNCTION	'A'-MUX SELECT	REG. CONTROL			CARRY		OUT EN	STATUS CNTRL	BUS		LED	SEQ CNTRL	BRANCH ADDRESS	F.B.
					'B'- REG	WLB	WHB	CIN	SX			CNTRL	G				
SOURCE	REG DIR	001 00000	B	BUS	RS	0	0	0	A7	0	NOP	NOP	0	0000	BR	0001	NOP
	WORD	00001	A	ACC	SRC	1	1	0	A7	0	NOP	NOP	0	0000	DONE	1111	NOP
	REG DIR	00010	B	BUS	RS	0	0	0	A7	0	NOP	NOP	0	0000	BR	0011	NOP
	BYTE	00011	A	ACC SX	SRC	1	1	0	A7	0	NOP	NOP	0	0000	DONE	1111	NOP
	REG A-DEC	00100	A+B	-2	RS	1	1	0	A7	0	NOP	NOP	0	0000	BR	0101	NOP
	WORD	00101	B	BUS	RS	0	0	0	A7	1	NOP	LAR	0	0000	DONE	1111	NOP
	REG A-DEC	00110	A+B+1	-2	RS	1	1	1	A7	0	NOP	NOP	0	0000	BR	0111	NOP
	BYTE	00111	B	BUS	RS	0	0	0	A7	1	NOP	LAR	0	0000	DONE	1111	DBE
	ABSOL	01000	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	1001	NOP
	WORD	01001	A	BUS	PC	0	0	0	A7	0	NOP	LAR	0	0000	DONE	1111	NOP
	ABSOL	01010	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	1011	NOP
	BYTE	01011	A	BUS	PC	0	0	0	A7	0	NOP	LAR	0	0000	DONE	1111	DBE
	IMMED	01100	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	DONE	1111	NOP
	WORD	01101															
	IMMED	01110	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	DONE	1111	NOP
	BYTE	01111															
	REG DEF	10000	B	BUS	RS	0	0	0	A7	1	NOP	LAR	0	0000	DONE	1111	NOP
	WORD	10001	A	ACC	SRC	1	1	0	A7	0	NOP	NOP	0	0000	BR	0011	NOP
	REG DEF	10010	B	BUS	RS	0	0	0	A7	1	NOP	LAR	0	0000	DONE	1111	DBE
	BYTE	10011	B	BUS	SRC	0	0	0	A7	1	NOP	LAR	0	0000	DONE	1111	NOP
	REG AI	10100	A+B+1	+1	RS	1	1	1	A7	1	NOP	LAR	0	0000	DONE	1111	NOP
	WORD	10101	A	ACC	SRC	1	1	0	A7	0	NOP	NOP	0	0000	BR	0111	NOP
	REG AI	10110	A+B	+1	RS	1	1	0	A7	1	NOP	LAR	0	0000	DONE	1111	DBE
	BYTE	10111	B	BUS	SRC	0	0	0	A7	1	NOP	LAR	0	0000	DONE	1111	DBE
	REL	11000	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	1001	NOP
	WORD	11001	A+B	BUS	PC	0	0	0	A7	0	NOP	NOP	0	0000	BR	0001	NOP
	REL	11010	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	1011	NOP
	BYTE	11011	A+B	BUS	PC	0	0	0	A7	0	NOP	NOP	0	0000	BR	0101	NOP
	INDEX	11100	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	1101	NOP
	WORD	11101	A+B	BUS	RS	0	0	0	A7	0	NOP	NOP	0	0000	BR	0001	NOP
	INDEX	11110	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	1111	NOP
	BYTE	11111	A+B	BUS	RS	0	0	0	A7	0	NOP	NOP	0	0000	BR	0101	NOP

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TABLE 2C

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MICRO-PROGRAM SYMBOLIC LISTING

MICRO ROUTINE	SUB BLOCK	BINARY ADDRESS	ALU FUNCTION	'A'-MUX SELECT	REG. CONTROL			CARRY		OUT EN	STATUS CNTRL	BUS		LED	SEQ CNTRL	BRANCH ADDRESS	F.B.
					'B'- REG	WLB	WHB	CIN	SX			CNTRL	G				
DESTINATION	REG DIR	010 00000	B	BUS	RD	0	0	0	A7	0	NOP	NOP	0	0000	DONE	1111	NOP
	WORD	00001															
	REG DIR	00010	B	BUS	RD	0	0	0	A7	0	NOP	NOP	0	0000	BR	0011	NOP
	BYTE	00011	A	ACC SX	TEMP	0	0	0	A7	0	NOP	NOP	0	0000	DONE	1111	NOP
	REG A-DEC	00100	A+B	-2	RD	1	1	0	A7	0	NOP	NOP	0	0000	BR	0101	NOP
	WORD	00101	B	BUS	RD	0	0	0	A7	1	NOP	LAR	0	0000	DONE	1111	NOP
	REG A-DEC	00110	A+B+1	-2	RD	1	1	1	A7	0	NOP	NOP	0	0000	BR	0111	NOP
	BYTE	00111	B	BUS	RD	0	0	0	A7	1	NOP	LAR	0	0000	DONE	1111	DBE
	ABSOL	01000	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	1001	NOP
	WORD	01001	A	BUS	PC	0	0	0	A7	0	NOP	LAR	0	0000	DONE	1111	NOP
	ABSOL	01010	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	1011	NOP
	BYTE	01011	A	BUS	PC	0	0	0	A7	0	NOP	LAR	0	0000	DONE	1111	DBE
	ABSOL DEF RD	01100	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	1101	NOP
	WORD	01101	A	BUS	PC	0	0	0	A7	0	NOP	LAR	0	0000	BR	1001	NOP
	ABSOL DEF RD	01110	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	1111	NOP
	BYTE	01111	A	BUS	PC	0	0	0	A7	0	NOP	LAR	0	0000	BR	1011	NOP
	REG DEF	10000	B	BUS	RD	0	0	0	A7	1	NOP	LAR	0	0000	DONE	1111	NOP
	WORD	10001	A	ACC	TEMP	1	1	0	A7	0	NOP	NOP	0	0000	BR	0011	NOP
	REG DEF	10010	B	BUS	RD	0	0	0	A7	1	NOP	LAR	0	0000	DONE	1111	DBE
	BYTE	10011	B	BUS	TEMP	0	0	0	A7	1	NOP	LAR	0	0000	DONE	1111	NOP
	REG AI	10100	A+B+1	+1	RD	1	1	1	A7	1	NOP	LAR	0	0000	DONE	1111	NOP
	WORD	10101	A	ACC	TEMP	1	1	0	A7	0	NOP	NOP	0	0000	BR	0111	NOP
	REG AI	10110	A+B	+1	RD	1	1	0	A7	1	NOP	LAR	0	0000	DONE	1111	DBE
	BYTE	10111	B	BUS	TEMP	0	0	0	A7	1	NOP	LAR	0	0000	DONE	1111	DBE
	REL	11000	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	1001	NOP
	WORD	11001	A+B	BUS	PC	0	0	0	A7	0	NOP	NOP	0	0000	BR	0001	NOP
	REL	11010	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	1011	NOP
	BYTE	11011	A+B	BUS	PC	0	0	0	A7	0	NOP	NOP	0	0000	BR	0101	NOP
	INDEX	11100	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	1101	NOP
	WORD	11101	A+B	BUS	RD	0	0	0	A7	0	NOP	NOP	0	0000	BR	0001	NOP
	INDEX	11110	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	1111	NOP
	BYTE	11111	A+B	BUS	RD	0	0	0	A7	0	NOP	NOP	0	0000	BR	0101	NOP

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MICRO-PROGRAM SYMBOLIC LISTING

MICRO ROUTINE	SUB BLOCK	BINARY ADDRESS	ALU FUNCTION	'A'-MUX SELECT	REG. CONTROL			CARRY		OUT EN	STATUS CNTRL	BUS		LED	SEQ CNTRL	BRANCH ADDRESS	F.B.
					'B'- REG	WLB	WHB	CIN	SX			CNTRL	G				
DESTINATION (cont'd)	REG DEF	01100000	B	BUS	RD	0	0	0	A7	0	NOP	NOP	0	0000	BR	0001	NOP
		00001	A	ACC	SRC	1	1	0	A7	0	NOP	NOP	0	0000	DONE	1111	NOP
		00010	A+B	ACC	PC	1	1	0	A7	0	NOP	NOP	0	0000	DONE	1111	NOP
DESTINATION (cont'd)	BRANCH	00011															
		00100	A+B	-2	RD	1	1	0	A7	0	NOP	NOP	0	0000	BR	0101	NOP
		00101	B	BUS	RD	0	0	0	A7	1	NOP	LAR	0	0000	BR	0110	NOP
		00110	A	BUS	SRC	1	1	0	A7	0	NOP	NOP	0	0000	DONE	1111	NOP
	REL	00111															
		01000	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	1001	NOP
		01001	A+B	BUS	PC	0	0	0	A7	0	NOP	NOP	0	0000	BR	0001	NOP
		01010															
		01011															
	INDEX DEF RD	01100	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	1101	NOP
		01101	A+B	BUS	RD	0	0	0	A7	0	NOP	NOP	0	0000	BR	1110	NOP
		01110	A	ACC	SRC	1	1	0	A7	0	NOP	NOP	0	0000	BR	1111	NOP
		01111	B	BUS	SRC	0	0	0	A7	1	NOP	LAR	0	0000	BR	0110	NOP
	ABSOL	10000	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	0001	NOP
		10001	A	BUS	SRC	1	1	0	A7	0	NOP	NOP	0	0000	DONE	1111	NOP
		10010	A-B-CIN	ACC	RS	1	1	C	A7	0	NOP	NOP	0	0100	BRZ=0	1110	NOP
		10011	A+A	-2	R2	1	1	0	A7	0	BUS	NOP	0	0100	BR	0110	NOP
	ABSOL DEF RD	10100	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	0101	NOP
		10101	A	BUS	PC	0	0	0	A7	0	NOP	LAR	0	0000	BR	0001	NOP
		10110	A+B	ACC	R1	1	1	0	A7	0	NOP	NOP	0	0100	BR	0111	NOP
		10111	A⊕B	ACC	RD	0	0	0	A7	0	NOP	NOP	0	0100	BRZ=1	1001	NOP
	REG AUTO IN	11000	A+B+1	+1	RD	1	1	1	A7	1	NOP	LAR	0	0000	BR	0001	NOP
		11001	B	ACC	RS	0	0	0	A7	0	NOP	NOP	0	1000	BR	1010	NOP
		11010	A+A+1	ACC	RS	0	0	1	A7	0	XFR	NOP	0	1000	BR	1011	NOP
		11011	A+A	ACC	RS	0	0	0	A7	0	NOP	NOP	0	1000	BR	1101	NOP
	TEST	11100	A	ACC SR	R2	1	1	0	A7	0	SHR	NOP	0	0100	BR	0010	NOP
		11101	A	ACC SX	RS	0	0	ACC15	C	0	NOP	NOP	0	1000	BR	1111	NOP
		11110	A	ACC	RS	0	0	0	A7	0	NOP	NOP	0	0100	DONE	1111	NOP
		11111	A	AC SWB	RS	0	0	0	A7	0	NOP	NOP	0	1000	DONE	1111	NOP

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MICRO ROUTINE	SUB BLOCK	BINARY ADDRESS	ALU FUNCTION	'A'-MUX SELECT	REG. CONTROL			CARRY		OUT EN	STATUS CNTRL	BUS		LED	SEQ CNTRL	BRANCH ADDRESS	F.B.
					'B'- REG	WLB	WHB	CIN	SX			CNTRL	G				
CTRL	SOFTWR TRAP	10000000	B	BUS	PC	0	0	0	A7	0	SET T	NOP	0	0000	BR	0001	NOP
		00001	A	ACC	TRAP	1	1	0	A7	0	NOP	NOP	0	0000	BR	0010	NOP
		00010	A+A	-2	SRC	0	0	0	A7	0	NOP	NOP	0	0000	BR	0011	NOP
		00011	A-B	ACC	SRC	1	1	1	A7	0	NOP	NOP	0	0000	BR	0100	NOP
	SOFTWR TRAP (CONT)	00100	A+B	-2	SRC	1	1	0	A7	0	NOP	NOP	0	0000	BR	0101	NOP
		00101	B	BUS	SRC	0	0	0	A7	1	NOP	LAR	0	0000	BR	0111	NOP
		00110	B	BUS	TRAP	0	0	0	A7	0	NOP	NOP	0	0000	BR	1111	NOP
		00111	A	BUS	PC	1	1	0	A7	0	NOP	NOP	0	0000	DONE	1111	NOP
	CCOPC	01000	A	ACC-SR	SRC	1	1	0	A7	0	NOP	NOP	0	0000	BR	1001	NOP
		01001	A∧B	STATUS	SRC	0	0	0	A7	0	BUS	NOP	0	0000	DONE	1111	NOP
		01010	B	BUS	TRAP	0	0	0	A7	0	CLRT	NOP	0	0000	BR	1011	NOP
		01011	A	ACC	PC	1	1	0	A7	0	NOP	NOP	0	0000	DONE	1111	NOP
	CCOP S	01100	A	ACC-SR	SRC	1	1	0	A7	0	NOP	NOP	0	0000	BR	1101	NOP
		01101	A∨B	STATUS	SRC	0	0	0	A7	0	BUS	NOP	0	0000	DONE	1111	NOP
		01110	B	BUS	TRAP	0	0	0	A7	0	CLRT	NOP	0	0000	BR	1111	NOP
		01111	A	ACC	PC	1	1	0	A7	0	NOP	NOP	0	0000	DONE	1111	S-TRAP
	RBT	10000	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	0001	NOP
		10001	A	BUS	SRC	1	1	0	A7	0	NOP	NOP	0	0000	BR	0010	NOP
		10010	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	0011	NOP
		10011	A	BUS	TEMP	0	0	0	A7	0	NOP	LAR	0	0000	BR	0100	NOP
	RBT (CONT)	10100	A	BUS	TEMP	1	1	0	A7	0	NOP	NOP	0	0000	BR	0101	NOP
		10101	A+B+1	+1	TEMP	1	1	1	A7	0	NOP	NOP	0	0000	BR	0110	NOP
		10110	A+B	-2	TEMP	1	1	0	A7	1	NOP	WWI	0	0000	BR	0111	NOP
		10111	B	BUS	TEMP	0	0	0	A7	1	NOP	LAR	0	0000	BR	1000	NOP
	RBT (CONT)	11000	A	BUS	TEMP	0	0	0	A7	0	NOP	LDA	0	0000	BR	1001	NOP
		11001	A+B+1	-2	SRC	1	1	1	A7	0	NOP	RDI	0	0000	BRZ=1	1011	NOP
		11010	A+B+1	-2	SRC	1	1	1	A7	0	NOP	RDI	0	0000	BRZ=0	1010	NOP
		11011	A	BUS	SRC	0	0	0	A7	0	NOP	NOP	0	0000	BR	1100	NOP
	RTI	11100	A+B+1	+1	SP	1	1	1	A7	1	NOP	LAR	0	0000	BR	1101	NOP
		11101	A	BUS	SP	0	0	0	A7	0	BUS	NOP	0	0000	BR	1110	NOP
		11110	A+B+1	+1	SP	1	1	1	A7	1	NOP	LAR	0	0000	BR	1111	NOP
		11111	A	BUS	PC	1	1	0	A7	0	NOP	NOP	0	0000	DONE	1111	NOP

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MICRO ROUTINE	SUB BLOCK	BINARY ADDRESS	ALU FUNCTION	'A'-MUX SELECT	REG. CONTROL			CARRY		OUT EN	STATUS CNTRL	BUS		LED	SEQ CNTRL	BRANCH ADDRESS	F.B.
					'B'- REG.	WLB	WHB	CIN	SX			CNTRL	G				
CONTROL (Cont'd)	LED 0	101 00000	A-1	ACC	SRC	0	0	0	A7	0	NOP	NOP	0	0001	BRZ=0	0000	NOP
		00001	B	BUS	SRC	0	0	0	A7	0	NOP	NOP	0	0001	DONE	1111	NOP
	SEARCH	00010	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	0011	NOP
		00011	A	BUS	SRC	1	1	0	A7	0	NOP	NOP	0	0000	BR	0100	NOP
	SEARCH (CONT)	00100	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	0101	NOP
		00101	A	BUS	TEMP	1	1	0	A7	0	NOP	NOP	0	0000	BR	0110	NOP
		00110	A^B	+1	RD	1	1	0	A7	0	XFR	NOP	0	0000	BRZ=1	1100	NOP
		00111	A+B	ACC	RO	1	1	0	A7	1	NOP	LDA	0	0000	BR	1000	NOP
	SEARCH (CONT)	01000	A	BUS	SRC	0	0	0	A7	0	NOP	RDI	0	0000	BR	1001	NOP
		01001	A^B	BUS	SRC	0	0	0	A7	0	NOP	NOP	0	0000	BR	1010	NOP
		01010	A+B	ACC	TEMP	0	0	0	A7	0	NOP	NOP	0	0000	BRZ=0	1101	NOP
		01011	A+B	-2	RD	1	1	0	A7	0	XFR	RDI	0	0000	BRZ=0	1001	NOP
	SEARCH (CONT)	01100	A+B	ACC	RO	1	1	0	A7	0	NOP	NOP	0	0000	DONE	1111	NOP
		01101	A-B-1	+1	RD	0	0	0	A7	0	NOP	NOP	0	0000	BR	1100	NOP
	LD TRAP	01110	B	BUS	RD	0	0	0	A7	0	SETT	NOP	0	0000	BR	1111	NOP
		01111	A	ACC	TRAP	1	1	0	A7	0	NOP	NOP	0	0000	DONE	1111	NOP
	LED 1	10000	A-1	ACC	SRC	0	0	0	A7	0	NOP	NOP	0	0010	BRZ=0	0000	NOP
		10001	B	BUS	SRC	0	0	0	A7	0	NOP	NOP	0	0010	DONE	1111	NOP
		10010															
		10011															
		10100															
		10101															
		10110															
		10111															
		11000															
		11001															
		11010															
		11011															
		11100															
		11101															
		11110															
		11111															

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MICRO ROUTINE	SUB BLOCK	BINARY ADDRESS	ALU FUNCTION	'A'-MUX SELECT	REG. CONTROL			CARRY		OUT EN	STATUS CNTRL	BUS		LED	SEQ CNTRL	BRANCH ADDRESS	F.B.
					'B'- REG.	WLB	WHB	CIN	SX			CNTRL	G				
CONTROL (Cont'd)	LED 2	110 00000	A-1	ACC	SRC	0	0	0	A7	0	NOP	NOP	0	0100	BRZ=0	0000	NOP
		00001	B	BUS	SRC	0	0	0	A7	0	NOP	NOP	0	0100	DONE	1111	NOP
	STORE	00010	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	0011	NOP
		00011	A	BUS	SRC	1	1	0	A7	0	NOP	NOP	0	0000	BR	0100	NOP
	STORE (CONT)	00100	A+B+1	+1	PC	1	1	1	A7	1	NOP	LAR	0	0000	BR	0101	NOP
		00101	A	BUS	TEMP	1	1	0	A7	0	NOP	NOP	0	0000	BR	0110	NOP
		00110	B	BUS	RO	0	0	0	A7	1	NOP	LAR	0	0000	BR	1101	NOP
		00111	A	ACC	X	1	1	0	A7	0	NOP	NOP	0	0000	BR	1001	NOP
SRC II	WORD	01000	A	BUS	SRC	1	1	0	A7	0	NOP	RDV	0	0000	DONE	1111	NOP
		01001	B	BUS	X	0	0	0	A7	1	NOP	WWI	0	0000	BR	1100	NOP
	BYTE	01010	A	BUS SX	SRC	1	1	0	A7	0	NOP	RDV	0	0000	DONE	1111	NOP
		01011	A	BSWBSX	SRC	1	1	0	A7	0	NOP	RDV	0	0000	DONE	1111	NOP
		01100	A+B	-2	RD	1	1	0	A7	0	NOP	RDW	0	0000	BRZ=1	0001	NOP
		01101	A^B	BUS	SRC	0	0	0	A7	0	NOP	NOP	0	0000	BR	1111	NOP
		01110	A	ACC SX	TEMP	0	0	ACC15	C	0	NOP	NOP	0	0000	DONE	1111	NOP
		01111	A^B	ACC	TEMP	0	0	0	A7	0	NOP	NOP	0	0000	BR	0111	NOP
CONTROL (Cont'd)	LED 3	10000	A-1	ACC	SRC	0	0	0	A7	0	NOP	NOP	0	1000	BRZ=0	0000	NOP
		10001	B	BUS	SRC	0	0	0	A7	0	NOP	NOP	0	1000	DONE	1111	NOP
	MOV IV REG	10010	B	BUS	IV	0	0	0	A7	0	NOP	NOP	0	0000	BR	0011	NOP
		10011	A	ACC	RD	1	1	0	A7	0	NOP	NOP	0	0000	DONE	1111	NOP
	WAIT	10100	A+B+1	-2	RD	1	1	1	A7	0	NOP	RDW	0	0000	BRZ=0	0100	NOP
		10101	A	BUS	RD	0	0	0	A7	0	NOP	NOP	0	0000	DONE	1111	NOP
	READ IV	10110	A+A	ACC SX	IV	0	0	0	A7	0	NOP	NOP	1	0000	BRZ=0	0110	NOP
		10111	A	BUS	IV	0	0	0	A7	0	NOP	NOP	1	0000	BR	1001	NOP
DST II	WORD	11000	A	BUS	TEMP	0	0	0	A7	0	NOP	RDV	0	0000	DONE	1111	NOP
		11001	A	BUS	IV	1	1	0	A7	0	NOP	RDV	1	0000	DONE	1111	NOP
	BYTE	11010	A	BUS SX	TEMP	0	0	0	A7	0	NOP	RDV	0	0000	DONE	1111	NOP
		11011	A	BSWBSX	TEMP	0	0	0	A7	0	NOP	RDV	0	0000	DONE	1111	NOP
	RORAWD	11100	A	BUS	TEMP	0	0	0	A7	0	NOP	RDV	0	0000	DONE	1111	NOP
		11101															
	RORABY	11110	A	BUS SX	TEMP	0	0	ACC15	C	0	NOP	RDV	0	0000	DONE	1111	NOP
		11111	A	BSWBSX	TEMP	0	0	ACC15	C	0	NOP	RDV	0	0000	DONE	1111	NOP

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MICRO ROUTINE	SUB BLOCK	BINARY ADDRESS	ALU FUNCTION	'A'-MUX SELECT	REG. CONTROL		CARRY		OUT EN	STATUS CNTRL	BUS		LED	SEQ CNTRL	BRANCH ADDRESS	F.B.
					'B'-REG	WLB	WHB	CIN	SX		CNTRL	G				
EXECUTE	SUB	11100000	A-B	ACC	SRC	1	1	1	A7	SUB	NOP	0	0000	DONE	1111	NOP
	MVP	000001	B	ACC	SRC	1	1	0	A7	XFR	NOP	0	0000	DONE	1111	NOP
	CMP	000010	A-B	ACC	SRC	1	1	1	A7	SUB	NOP	0	0000	DONE	1111	NOP
	BIT	000011	A^B	ACC	SRC	1	1	0	A7	XFR	NOP	0	0000	DONE	1111	NOP
	BIC	001000	A^B	ACC	SRC	1	1	0	A7	XFR	NOP	0	0000	DONE	1111	NOP
	BIS	001001	A^B	ACC	SRC	1	1	0	A7	XFR	NOP	0	0000	DONE	1111	NOP
	XOR	001010	A^B	ACC	SRC	1	1	0	A7	XFR	NOP	0	0000	DONE	1111	NOP
	ADD	001011	A+B	ACC	SRC	1	1	0	A7	ADD	NOP	0	0000	DONE	1111	NOP
	CLR	010000	0	ACC	SRC	1	1	0	A7	XFR	NOP	0	0000	DONE	1111	NOP
	COM	010001	A	ACC	SRC	1	1	0	A7	XFR	NOP	0	0000	DONE	1111	NOP
DATA	JNC	010100	A+1	ACC	SRC	1	1	1	A7	XFR	NOP	0	0000	DONE	1111	NOP
	DEC	010101	A-1	ACC	SRC	1	1	0	A7	XFR	NOP	0	0000	DONE	1111	NOP
	TST	011000	A	ACC	SRC	1	1	0	A7	XFR	NOP	0	0000	DONE	1111	NOP
	ASL	011001	A+A	ACC	SRC	1	1	0	A7	ADD	NOP	0	0000	DONE	1111	NOP
	ASR	011010	A	ACC	SRC	1	1	ACC15	C	SHR	NOP	0	0000	DONE	1111	NOP
	RDL	011011	A+A+CIN	ACC	SRC	1	1	C	A7	ADD	NOP	0	0000	DONE	1111	NOP
	WORD	100000	B	BUS	SRC	0	0	0	A7	NOP	WWT	0	0000	DONE	1111	NOP
	BYTE	100001	B	BUS	SP	0	0	0	A7	NOP	LDA	0	0000	BR	0101	NOP
	QDDBY	100010	B	BUS	SRC	0	0	0	A7	NOP	WBI	0	0000	DONE	1111	NOP
	DM*WD	100011	A	ACC	SRC	0	0	0	A7	NOP	NOP	0	0000	BR	0010	NOP
EXECUTE (CONT)	DM*BY	101000	A	ACC	RD	1	1	0	A7	NOP	NOP	0	0000	DONE	1111	NOP
	RQR	101001	B	BUS	PC	0	0	0	A7	NOP	WWT	0	0000	BR	0111	NOP
	SWAB	101010	A	ACC	RD	1	1	0	A7	NOP	NOP	0	0000	DONE	1111	NOP
	TSR	101011	A	STATUS	SRC	0	0	0	A7	NOP	NOP	0	0000	DONE	1111	NOP
	TTR	110100	B	ACC	TRAP	0	0	0	A7	NOP	NOP	0	0000	BR	1100	NOP
		111000	A	ACC	SRC	1	1	0	A7	NOP	NOP	0	0000	DONE	1111	NOP
		111001	A	ACC	SRC	0	0	0	A7	NOP	NOP	0	0000	DONE	1111	NOP
		111010	A	ACC	PC	1	1	0	A7	XFR	NOP	0	0000	DONE	1111	NOP
		111011	A	ACC	PC	1	1	0	A7	NOP	NOP	0	0000	DONE	1111	NOP
	JMP	111100	A+B	-2	SP	1	1	0	A7	NOP	NOP	0	0000	BR	0001	NOP

4.7.1 Example of microprogram sequencing.

All executions of macro-instructions begin in the FETCH microroutine, or major state. Normal entry into FETCH is made at address 2 (octal) if no interrupts, traps or tests are pending. The following control sequence is generated.

At Address 2 - Place the constant 000001 (octal) on the A operand bus, and register PC (program counter) on the B operand bus. Perform the ALU operation A+B+1, causing PC+2 to be generated at the output of the ALU. Place the contents of the B operand bus (PC) onto the TELEBUS and generate a "Load-Address-and-read" command via the bus controls. Write the contents (PC+2) of the ALU output back into both bytes of the PC register. Clear any previous "odd byte" condition and branch to microprogram address 3.

At Address 3 - Sign extend bit A7 of the TELEBUS contents (result of previous LAR) and place it on the A operand bus. Perform the ALU operation A+A; this operation shifts the operand left (multiplies by 2). Write the contents of the ALU output into both bytes of the SRC register. Also load the contents of the TELEBUS into the macro-instruction register of IXL/B. The microroutine is DONE at this point, and an entry into the next state microroutine is executed. The address of the next microroutine is generated by the next state address encoding logic and depends on the type of instruction which has been clocked into the instruction register. The above IXL/A operations are done in case the instruction clocked into the instruction register happens to be a BRANCH; in this case the correct branch offset has been placed in the SRC register, and is used later in the BRANCH microroutine. If the upcoming instruction is not a BRANCH, the contents of the SRC register are later ignored. For this example, we will assume the instruction is an "ADD R1, R2" (not a BRANCH). The decoding of this instruction by the IXL/B logic causes a next state address generation of 40 (octal), which is the address of the REG DIR sub-block of the SOURCE microroutine.

At Address 40 - Place the contents of the R₃ register (the register designated by IR6-IR8) on the B operand bus. Transfer the B operand through the ALU and into the accumulator (the output of the ALU is always clocked into the accumulator). Branch to microprogram address to address 41.

4.7.1 Continued

- At Address 41 - Place the contents of the accumulator onto the A operand bus, transfer through the ALU and write into both bytes of the SRC register (this register is used to hold the source operand until execution of the arithmetic operation). The microroutine is DONE at this point. The address encoding logic generates a next state address of 100 (octal); this corresponds to the REG DIR sub-block of the DESTINATION microroutine.
- At Address 100 - Place the contents of the R_D register (the register designated by IR_0 - IR_2) on the B operand bus. Transfer the B operand through the ALU and into the Accumulator. The DESTINATION microroutine is DONE at this point. The address encoding logic generates a next state address of 347 (octal); this corresponds to the ADD sub-block of the EXECUTE microroutine.
- At Address 347 - Place the contents of the accumulator on the A operand bus, and the contents of the SRC register on the B operand bus. Perform the operation $A+B$ in the ALU and write the results back into both bytes of the SRC register. The EXECUTE microroutine is DONE at this point, and the next state address encoding logic generates an address of 364 (octal). This corresponds to the DMO WD sub-block of the DATO microroutine.
- At Address 364 - Place the contents of the accumulator on the A operand bus and transfer it through the ALU. Write the result back into both bytes of the R_D register. The DATO microroutine is DONE at this point. A next state address of 2, 4, 10 or 20 is generated to reinitiate the FETCH routine in the normal, interrupt, trap or test modes respectively.

Thus the "ADD R_1 , R_2 " instruction requires 7 micro-steps or 7×1.12 or 7.84 microseconds.

4.8 FS-7 Timing Logic and Restart Timer

4.8.1 General

4.8.1.1 The Timing Logic within the IXL/B card assembly generates seven waveforms to synchronize the operation of 40C400 Controller. Three of the waveforms are Telebus signals, namely I/O Clock, Bus Enable, and Memory Clock. The four remaining waveforms are used by the IXL, namely Microprogram Clock (MP CLK), Interrupt Grant Clock (IG CLK), Accumulator Clock (ACC CLK), and Write Pulse.

4.8.1.2 The Timing Logic normally operates with a period of 1.116 Microseconds for all waveforms. The Logic deviates from this period when the Telebus command is to read from a device and when the Controller is running under standby power. When reading from a device, the I/O Clock is maintained at a period of 1.117 μ S. with the six other waveforms changed to 2.232 μ S. for one period only. Under standby power, the Timing Logic generates only the I/O CLK waveforms at a period 17.856 μ S.

The Timing Logic automatically change modes when the read from device command (RDV) is instituted by the microprogram or when the power switches to standby operation.

4.8.1.3 The timing waveforms are derived from the Crystal Oscillator (XTAL OSCILLATOR) oscillating at 14.336 MHz. with a period of 69.75 Nanoseconds.

4.8.1.4 The waveforms have a period of 1.116 Microseconds phased in increments of 69.75 μ S. To obtain the 1.116 μ S. period, the XTAL OSCILLATOR drives two divide-by-16 counters, the XCLK Counter (XCLK CNTR) and the Timing Ring Counter (TR CNTR). The XCLK CNTR is a four stage binary counter; the fourth stage generates I/O CLK. The TR CNTR is an eight stage twisted ring counter and generates six of the seven waveforms. Synchronization of the two counters and suppression of unwanted ring counter counting modes is the function of the TF Synchronizer gate.

4.8.1.5 Ten two input NAND and NOR gates decode the outputs of the TR CNTR and produce the Bus Enable, Memory Clock, MP CLK, IG CLK, ACC CLK and the Write Pulse.

4.8.1.6 To change the period of the six waveforms during a Read From Device (RDV) Telebus command, the RDV command is decoded from Telebus leads C_0 , C_1 , C_2 . The RDV DECODE circuit decodes the command. A signal RDV EN is generated within the IXL/B whenever DEVICE A ENABLE or DEVICE B ENABLE is actuated and is used with the RDV DECODE to trigger the "pulse stretching" of all timing signals except for the I/O CLK.

4.8.1.7 Provisions have been made to maintain +5V power to the XTAL OSCILLATOR and those integrated circuit packages which generate the I/O CLK when a set is equipped with a secondary power source. When power fails, the +5V Standby is to continue operation from the secondary source. During power failure, the I/O counter (I/O CNTR) is enabled and divides the I/O CLK by sixteen. During standby operation, the I/O CLK is active low on the Telebus for 17.3 μ S. and becomes high for 0.56 μ S. When normal power is restored, the I/O CNTR becomes passive and the I/O CLK returns to a period of 1.116 μ S.

4.8.1.8 The Restart Timer is an analog timing circuit that actuates the INITIALIZE Telebus lead. The momentary closing of a remote Restart switch is differentiated by an R-C circuit to trigger the Restart Timer. In turn the Timer drives the INITIALIZE lead to a Low level for 50 milliseconds.

4.8.1.9 Refer to 4401SD-9 for the schematic of the Timing logic and 4401SD-10, -11 and -12 for the Timing Charts TC1, TC2, TC3 and TC4.

4.8.2 Supporting Information

4.8.2.1 Schematic 4401SD

4.8.3 Crystal Oscillator and Multiplexer

4.8.3.1 The Crystal Oscillator (XTAL OSCILLATOR) is contained in one hybrid circuit package, MLC1. The output drives a two input multiplexer (MLC2) normally selected to the XTAL OSCILLATOR. The multiplexer output (MLC2-(4)) is XCLK, the basic clock signal for the timing generation.

4.8.3.2 The multiplexer MLC2 is used to replace the XTAL OSCILLATOR signal with an external source during production card testing or during use of a Test Panel. In normal operation, the signal leads OSC EN and MUX EN are held at a High voltage level by the resistors R4 and R6 connected to +5V Standby supply. To insert an external frequency source, the signal lead MUX EN (B3) is driven to a low level by external circuitry. The external frequency source is then connected to the signal lead OSC EN (B2). The multiplexer MLC2 selects the external source to become the signal XCLK.

4.8.3.3 The XTAL OSCILLATOR, package MLC2, and resistors R4 and R6 are powered from the +5V Standby supply. In standby operation, the signal XCLK is not interrupted.

4.8.4 XCLK Counter

4.8.4.1 The XCLK Counter, MLB1, is a four stage binary counter driven by the signal XCLK. The output of the last stage, MLB1-(11) is titled I/O CLK and is a square wave of frequency 896 kHz. Another XCLK CNTR output MLB1-(15) is entitled XCLK CNTR CARRY.

4.8.4.2 The time relationship of the XCLK Counter input and outputs are shown in TC-1 (4401SD-11) and TC-2 (4401SD-12). The signal CLK I/O is shown to be a sub-multiple of the XCLK frequency. The signal XCLK CNTR CARRY becomes active HIGH for one XCLK period prior to the HIGH TO LOW transition of the CLK I/O signal. In turn XCLK CNTR CARRY acts as a clock for the RDV Sequence Control.

4.8.4.3 The XCLK CNTR is powered from the +5 Volt Standby supply. The unused control leads of the SCLK CNTR is held HIGH by the resistor R2 and R3, connected also to +5 Volt Standby.

4.8.5 Timing Ring Counter

4.8.5.1 The Timing Ring Counter (TR CNTR) generates all timing waveforms except for I/O CLK. The division of timing signals is to allow standby or battery operation, and to allow a one cycle pause during Read from Device (RDV) Telebus operation. The I/O CLK signal is never interrupted while the TR CNTR outputs may be interrupted.

4.8.5.2 The Timing Ring Counter (TR CNTR) is an eight stage twisted ring counter composed of MLA2 and MLA1 integrated circuit packages. A twisted ring counter consists of a shift register with the output of the last stage inverted and connected to the first stage input. The TR CNTR consists of 8 D-Type flip-flops connected in series. The TF Synchronizer gate, MLB3, inverts the last stage output, TF7, and drives the first stage input, MLA2-(4).

4.8.5.3 The output signals of the TR CNTR are symmetrical pulses and are the 16th submultiple of CLK. The timing diagram TC-1 (4401SD-11) shows the TR CNTR outputs (TF0 through TF7); each output is displaced one XCLK period from the preceding output. Note that the TF Synchronizing gate synchronizes the TR CNTR with the I/O CLK signal, MLB1-(11), by gating or blocking the first stage input, MLB3-(4). In effect, the I/O CLK signal being in phase slows the TF signal.

4.8.6 Counter Decoders

4.8.6.1 The outputs (TF0 through TF7) are decoded by two input NOR and NAND gates to generate the required timing signals. The signals are generated as follows:

$$4.8.6.1.1 \quad \overline{\text{MEM CLK}} = \text{TF3} \wedge \overline{\text{TF6}}$$

$$4.8.6.1.2 \quad \text{IG CLK} = \overline{\text{TF0}}$$

$$4.8.6.1.3 \quad \text{ACC CLK} = \overline{\overline{\text{TF0}} \wedge \overline{\text{TF3}}}$$

$$4.8.6.1.4 \quad \overline{\text{BUS EN}} = \text{TF2}$$

$$4.8.6.1.5 \quad \text{MP CLK} = \text{TF4} \vee \overline{\text{TF3}}$$

$$4.8.6.1.6 \quad \text{WRITE PULSE} = \overline{\overline{\text{TF4}} \vee \overline{\text{TF3}}}$$

4.8.6.2 The I/O CLK signal is derived through three stages of inversion, MLC3-(11), MLC3-(8) and MLC3-(6). A signal I/O CLK ENABLE is used to gate I/O CLK during standby operation. The integrated circuit package MLC3 is powered from +5 Volt Standby.

4.8.7 RDV Decode and RDV Sequence Control

4.8.7.1 The RDV Decode and RDV Sequence Control logic detects the RDV command coincident with either DEVA EN or DEVB EN Telebus signals and proceeds to stop the TR CNTR for one bus cycle of 1.116 Microsecond. The pause is to allow response of slower I/O devices attached to the Telebus.

4.8.7.2 The RDV Decode gate decodes the Telebus controls generated by the Microprogram Storage Arrays MPC0, MPC1, MPC2. The MLA4-(12) lead goes HIGH for RDV detected. The signal RDV EN is generated whenever either Telebus DEV ENABLE signal is propagated. The coincidence of MLA4-(12) and RDV EN sets the FF0 flip-flop when the CLK CTR CARRY LOW to HIGH transition occurs. In turn the RDV FF0 goes LOW which clears MLA2 and stops the TR CNTR. At the same transition, RDV FF1 is set to 1, MLA3-(15) = HIGH, blocking the RDV FF0 input. The next LOW to HIGH transition of XCLK CTR CARRY will clear RDV FF0 allowing TR CNTR to commence counting.

4.8.7.3 The timing relationship of the RDV sequence is shown in TC-2 (4401SD-12). The XCLK CNTR CARRY is the synchronizing or clocking signal that sequences the RDV pause.

4.8.8 I/O Counter

4.8.8.1 For operation under standby conditions, a clock is required operating at a lesser frequency than normal operation. The clock is to exercise the dynamic memories to retain the stored data. The IXL provides the I/O CLK during standby or battery operation operating at 56 KHz. The I/O Counter (I/O CTR) provides the logic and counting to generate the sub-multiple I/O CLK.

4.8.8.2 During normal operation, the I/O CTR (MLC4) is held at count 15. Since I/O CTR is a four stage counter, the carry output (I/O CLK ENABLE) is always HIGH, thereby enabling MLC3-(18) and allowing I/O CLK to propagate through MLC3-(6) to the Telebus. The I/O CTR is held at count 15 by loading each flip-flop with logic 1 at each X CLK CTR CARRY cycle. The load signal, MLC4-(9), is derived from a NAND gate MLB2-(8), with the inputs, MLB2-(9,10) held HIGH by resistor R1. When power fails the signal MLB2-(8) previously LOW becomes HIGH. When clocked through the flip-flop MLA3-(10) to synchronize the signal, the load command MLC4-(9) goes HIGH. The I/O CTR proceeds to count and the I/O CLK ENABLE goes LOW blocking I/O CLK in a LOW state. Every 16 counts the I/O CLK ENABLE goes HIGH for one XCLK CTR CARRY cycle.

4.8.8.3 The timing diagram for standby power operation is shown in TC-3 (4401SD-13). The XCLK CTR CARRY becomes the synchronizing or clocking signal by controlling the ENP, MLC4-(7) lead of the I/O CTR. Note that the I/O CLK signal is the only Telebus signal defined for standby operation.

4.8.8.4 To remain in operation during standby conditions, the integrated circuit packages MLA3, MLB1, MLC1, MLC2, MLC3 and MLC4 are powered from the +5 Volt Standby supply.

4.9 Restart Timer

4.9.1 The Restart Timer is used to momentarily actuate the Telebus INITIALIZE to a low state for approximately 50 milliseconds. A HIGH to LOW transition at the input, RESTART (B55), is differentiated by the circuit of R16, R17 and C28 to trigger the timer, MLC18, with a HIGH to LOW pulse. Once triggered the timer output, POR, is actuated HIGH for approximately 50 milliseconds. The POR signal is inverted and drives the INITIALIZE lead LOW by the bus transceiver MLC5.

4406CD

CIRCUIT DESCRIPTION OF THE 410406 SSI INPUT/OUTPUT CIRCUIT CARD ASSEMBLY

SHEET 1

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TC482-1272

4406CD
Sheet 2
Issue 1

CIRCUIT DESCRIPTION OF THE
410406 SSI INPUT/OUTPUT CIRCUIT
CARD ASSEMBLY

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SECTION I - USER INFORMATION

1. General Description

1.01 The 410406 SSI (Standard Serial Interface) Input/Output Circuit Card Assembly provides the 40C400 Controller with four (4) interfaces to Model 40 line equipment requiring an SSI compatible interface. The four interface ports are partially comprised of Teletype MOS integrated circuits.

1.02 To interface the 40C400 Controller to the device being serviced, the MOS circuitry converts data and control information from the line discipline of the Telebus to the SSI compatible interface. The exchange of information is accomplished by the operating program in the controller reading or writing data into registers located in the MOS circuitry.

The parallel to serial conversion of the data to be transmitted is performed within the MOS circuitry by a Transmitting Concentrator. Four (4) eight (8) Bit registers are associated with the Transmitting Concentrator, two used to assemble the sixteen (16) Bit data word sent to the device and two used to assemble the thirteen (13) Bit control word sent to the device. One of the control registers contains three status bits of information to indicate the state of the data word register, the state of the control word register and an Enable Bit used to allow an interrupt request when the contents of the data word registers have been loaded into the Transmitting Concentrator. The operating program has a full word time (~ 320 u sec) to service the interrupt request and load the two data word registers with the next word to be sent should contiguous data word operation be desired.

The serial to parallel conversion of the incoming SSI word is performed within the MOS circuitry by a Receiving Distributor. Four (4) eight (8) Bit registers are associated with the Receiving Distributor, two used to store the sixteen (16) Bit data word received from the device and two used to store the ten (10) Bit status word received from the device. One of the status registers has six (6) local status and control bits which may under program control, (a) enable an interrupt request when a status word is received, (b) enable an interrupt request when a data word is received, (c) initiate a port test by causing the SSI send data to loop back to the SSI receive data, (d) indicate if an SSI Clock is present on the receive data verifying the existence of the remove device, (e) reflect the state of the data word registers and (f) inform the operating program that a data word has been received without the previous word being read. The operating program has a full word time (~320 u sec) to service the data and status registers without allowing an overwrite condition to exist.

2. Switch Options

2.01 The SSI Input/Output Circuit Card Assembly uses the lesser significant eight (8) bits of the sixteen (16) bit Data/Address Bus of the Telebus. Address bits A6 and A7 are switch programmable with Address bits A4 and A5 being determined by position of the port on the circuit card assembly. The additional address information (A8-A15) determined by Device A Enable (IOA) and Device B Enable (IOB) are switch programmable. The polarity of the most significant of the eight (8) bit interrupt vector and the magnetic tape options are also switch programmable.

The switches are located in one switch pack (SPB13) in the lower right hand corner of the card assembly as viewed from the component side.

SWITCH OPTIONS DEFINITIONS

- Switch 1 IOA/IOB/Vector Block - Selects one of two groups of device addresses (A8-A15) and determines polarity of Interrupt Vector Block
On = Closed = IOB = 1 for Bit 8 of Vector
Off = Open = IOA = 0 for Bit 8 of Vector
- Switch 2 Card Address A6
On = 0 for A6
Off = 1 for A6
- Switch 3 Card Address A7
On = 0 for A7
Off = 1 for A7
- Switch 4 Magnetic Tape Option Port A = The recording format of the Model 40 Magnetic Tape Cassette requires the SSI word time to be 22 SSI bits long (392,854 us). Thus a 4 bit stop must be added to the normal 18 bit frame.
On = Option In (22 bit word)
Off = Normal (18 bit word)

Switch 5 Magnetic Tape Option Port B - See above

Switch 6 Magnetic Tape Option Port C - See above

Switch 7 Magnetic Tape Option Port D - See above

3. Supporting Information

3.01 SSI Word Definition

The SSI Signalling Scheme utilizes a Di-Phase Clock for Data Interchange. At the transmission rate of 56 KBS, the base bit width is 17.857 usec and the alternate bit width is 8.928 usec. A mark is defined as one base bit, 17.857 usec wide, and a space is defined as two contiguous and opposite polarity 8.928 usec wide bits.

The data link is established when a Di-Phase "Mark" is present on both the transmitting leg ITD (to Device) and the receiving leg ITC (Device to Controller). Once the data link is established, information interchange may be initiated by either the 40C400 Controller to the device (through the SSI port) or from the device to the 40C400 Controller (through the SSI port).

The basic SSI word consists of four parts (1) Start (2) Steer, (3) Low Byte b0-b7, and (4) High Byte b8-b15. When sending to the device from the 40C400 Controller the start and steer bit is generated by the SSI port when the low byte (b0-b7) of the word is received from the 40C400 Controller. Thus if you want to update the data in the high byte only to the device, you must load the lower byte with the same byte information that was sent before.

3.02 Interrupt Vectors

Three interrupt vectors can be generated by each SSI port which are controlled by the 40C400 Controller via the correct enable bits.

Interrupt Name	Vector Address
A) Send Registers Empty	AX ₇ X ₆ X ₅ X ₄ 010
B) Data Word Received	AX ₇ X ₆ X ₅ X ₄ 110
C) Status Word Received	AX ₇ X ₆ X ₅ X ₄ 100

where A = IOA/IOB/Vector Block Switch Option
X₇X₆X₅X₄ = Card Address and Port Position Options (A7A6A5A4)

the enable bits for the interrupt vectors are:

Interrupt Name	Register Address	Bit Location
A) Send Register Empty	AX ₇ X ₆ X ₅ X ₄ 0010	5
B) Data Word Received	AX ₇ X ₆ X ₅ X ₄ 1010	6
C) Status Word Received	AX ₇ X ₆ X ₅ X ₄ 1010	7

3.03 Register Address Information

Each SSI port has eight (8) eight (8) bit registers, four (4) used to the device and four (4) used from the device. The register names and addresses are:

Register Name	From/To Device	Address
1) Control Low Byte	To	AX7X6X5X40000
2) Control High Byte	To	AX7X6X5X40010
3) Data Low Byte	To	AX7X6X5X40100
4) Data High Byte	To	AX7X6X5X40110
5) Status Low Byte	From	AX7X6X5X41000
6) Status High Byte	From	AX7X6X5X41010
7) Data Low Byte	From	AX7X6X5X41100
8) Data High Byte	From	AX7X6X5X41110

3.04 Register Bit Definitions

3.04.1 Control Register (Low Byte Controller to Device) - AX7X6X5X40000

BITS DESCRIPTION

- 0 INIT - Reserved for all SSI ports as the initialize signal and defined as device reset to its initial condition. This bit is Read/Write.
- 1 Send Status - is reserved for all devices as the command from the 40C400 Controller to send to the Controller the current contents of the device status register. This bit is Read/Write.
- 2 Test - Reserved for all SSI ports as the test signal causing the device to initiate an internal test, and upon completion of this test notify the 40C400 Controller, via the Status Register, the state of the test. This bit is Read/Write.
- 3-7 Unassigned - Device dependent. These bits are Read/Write.

3.04.2 Control Register (High Byte Controller to Device) - AX7X6X5X40010

BITS DESCRIPTION

- 0-4 Unassigned - Device dependent. These bits are Read/Write.
- 5 Send Data Interrupt Enable - This bit being set to a 1 and a full empty transition of the data registers, (Data (Low Byte) and Data (High Byte) loaded into the transmitting concentrator initiates the Send Data Interrupt Request. This bit is Read/Write.
- 6 Control Buffer Empty - This bit indicates the state of the Control Buffer. 1 = Empty, 0 = Full (waiting to be loaded into the Transmitting Concentrator). This bit is set to 1 when the data is loaded into the Transmitting Concentrator. This bit is Read Only.

- 7 Data Buffer Empty - This bit indicates the state of the Data Buffer 1 = Empty, 0 = Full (waiting to be loaded into the Transmitting Concentrator. This bit is set to 1 when the data is loaded into the Transmitting Concentrator. This bit is Read Only.

NOTE: Bits 5, 6 and 7 are used for information between the SSI port and the 40C400 Controller only. A mark is always sent in these three bit positions to the device being serviced.

3.04.3 Transmit Data Register (Low Byte Controller to Device) - AX7X6X5X40100

BITS DESCRIPTION

- 0-7 Data These bits are Write Only.

3.04.4 Transmit Data Register (High Byte Controller to Device) - AX7X6X5X40110

BITS DESCRIPTION

- 0-7 Data These bits are Write Only.

3.04.5 Status Register (Low Byte Device to Controller) - AX7X6X5X41000

BITS DESCRIPTION

- 0-7 Unassigned (from Device) These bits are Read Only

3.04.6 Status Register (High Byte Device to Controller and Local Status on Card) - AX7X6X5X41010

BITS DESCRIPTION

- 0-1 Unassigned (from device). These bits are Read Only.
- 2 SSI Line Status - This bit reflects the SSI line condition as to the presence of the Di-Phase clock. (1 = Clock on, 0 = Clock off). A change of the state of the clock initiates a Status Received Interrupt Vector if the Status Interrupt Enable Bit is Set to 1. This bit is Read Only.
- 3 Data Word Available - This bit being a 1 indicates that a data word has been received from the device and is available at AX1X2X3X41100 and AX1X2X3X41110. The receiving of the data word from the device will cause a Data Received Interrupt Vector, if the Data Interrupt Enable bit is set to 1. This bit is Read Only.
- 4 Overflow - This bit indicates the state of the input data buffer. (Device to Controller) Should a data word be received from the device without the prior one having been accessed this bit will set to a 1. This bit can be cleared to a zero only by the 40C400 Controller. This bit is Read/Write 0.

<u>BITS</u>	<u>DESCRIPTION</u>
5	<u>Loopback</u> - This bit initiates the loopback test mode, connecting the Transmitting Concentrator to the Receiving Distributor. The data to the device is held in the marking condition and all input data from the device is ignored. Loopback = 1, Normal = 0 This bit is <u>Read/Write</u> .

NOTE: Care must be taken when switching in and out of loopback that a character is not being sent by the Transmitting Concentrator (wait a minimum of 321.6 us from last loading of Transmitting Concentrator).

<u>BITS</u>	<u>DESCRIPTION</u>
6	<u>Status Interrupt Enable</u> - This bit having been set to a one, and a status word is received from the device or the SSI Line Status changes will generate the Status Received Interrupt vector request. 1 = Enable, 0 = Not Enabled. This bit is <u>Read/Write</u> .
7	<u>Data Interrupt Enable</u> - This bit having been set to a one, and a Data Word is received from the device. The Data Received Interrupt Vector will be generated. 1 = Enable, 0 = Not Enabled. This bit is <u>Read/Write</u> .

3.04.7 Input Data (Low Byte Device to Controller) - AX7X6X5X41100

<u>BITS</u>	<u>DESCRIPTION</u>
0-7	<u>Data</u> (from Device). These bits are <u>Read Only</u> .

3.04.8 Input Data (High Byte Device to Controller) - AX7X6X5X41110

<u>BITS</u>	<u>DESCRIPTION</u>
0-7	<u>Data</u> (from Device). These bits are <u>Read Only</u> .

3.05 Signal Designation

Signal leads are labeled with a title descriptive of the function of the signal. A line may or may not be drawn over this title, indicating that the signal is in the low or high state respectively when the state described by the title of the signal is present.

3.06 Voltage Requirements

3.06.1 The voltages required by the 410406 Card Assembly have the following tolerances:

<u>Voltage</u>	<u>Voltage Range</u>
+5V	+4.5V to +5.5V
-12V	-10.8V to -13.2V
+12V	+10.8V to +13.2V

3.06.2 Other voltages referred to in the circuit description have the following tolerances:

<u>Voltage</u>	<u>Voltage Range</u>
V _L	0.0V to +0.8V
V _H	+2.4V to +5.5V
V _{LM}	-1.0V to +0.8V
V _{HM}	+9.5V to +13.2V

SECTION II - CIRCUIT DESCRIPTION

1. General Description - with Block Diagram

The SSI Input/Output Block Diagram of Figure 1 shows the relationship between the various functional blocks (FS-1 to FS-7).

Data/Address information from the Telebus and Data, status and interrupt vector information from the four (4) SSI ports to the Telebus pass through FS-2. Eight bit data/address from the Telebus passes into either the Transmit Data Interface (FS-4) or the Receive Data Interface (FS-5). Data and vector address information return from FS4 and FS-5 to FS-2. Control, timing and interrupt control signals from the Telebus to the SSI ports pass through FS-3 to drive FS-4, FS-5, FS-6 and FS-7.

The Receive Distributor with associated registers, the Transmitting Concentrator with associated registers and all other pertinent circuitry are contained within the MOS circuitry and are depicted simply as functional elements.

For more detailed information regarding the MOS circuitry refer to Specification 344979S and 344981S.

Power distribution, decoupling and receiver enabling is performed in FS-1.

2. Detailed Description

2.01 FS-1 (Power Distribution and Shielding)

2.01.1 General - Functional Block FS-1 provides the distribution of power, high frequency decoupling of the regulated power signals, signal shielding at the Telebus connector and the Telebus receiver enabling.

2.01.2 Capacitors C1 and C9-C11 provide high frequency decoupling of the +5V Power lead to ground. The decoupling is accomplished by presenting a relatively low impedance to high frequency signals on the decoupled lead. Capacitors C12 and C13 decouple -12V and +12V respectively to ground. Capacitors C2-C8 decouple +12V to -12V.

2.01.3 Telebus receivers MLD1, MLD2 and MLD3 are always enabled by connecting the respective disables OFF (V_L).

2.01.4 The Telebus signal shields are connected to ground for the shielding function.

2.02 FS-2 (Data/Address Splitting and Level Shifting).

2.02.1 General - Functional Block FS-2 performs the transceiver function for the eight (8) Data/Address Telebus signals.

2.02.2 High impedance receivers (MLD2 and MLD3) operate in conjunction with open-collector drivers (MLA2 and MLA3) to accomplish the transceiver operation.

2.02.3 The level shifting of the TTL compatible Telebus to the MOS voltage levels are accomplished by high voltage open collector drivers (MLB2 and MLB3) with 1K resistors providing the V_{HM} levels. The level shifting of the MOS levels to the Telebus levels is accomplished by a voltage divider network (series resistors on FS-4 and FS-5) with resistors to -12V in such a ratio to guarantee V_H into MLA2 and MLA3 with V_{HM} into the divider, and V_L when the MOS allows the divider input to float. The 6.8K resistors to -12V assure sufficient current sinking to guarantee V_L into MLA2 and MLA3. The bi-directional Data/Address of the Telebus is thus split to MOS compatible voltage Data/Address to the SSI ports and Data from the SSI ports. MLA2 and MLA3 are disabled by INENBS (INENB) to force the proper release timing for the Telebus data.

2.03 FS-3 (Control and Interrupt Logic Level Shifting)

2.03.1 General - Functional Block FS-3 performs the Telebus to MOS compatible level interface for the control leads and the interrupt signals. A divider network generates the clock signal to the transmit concentrator.

2.03.2 High impedance receivers (MLD1 and MLD2) provide the direct interface from the Telebus and operate in conjunction with open collector high voltage drivers (MLB2 and MLC2) to generate the MOS compatible levels, with 1K resistor providing the V_{HM} levels.

2.03.3 Switch option 1 in conjunction with MLD4 exclusively select I/OA or I/OB and form the I/O SELECT signal which enables the four SSI ports. The VBOPT signal reflects the state of switch option 1.

2.03.4 The 4-bit counter, MLC1, divides the I/O CLK (896KHz) to 112KHz to be used by the send portion of the SSI port.

2.03.5 The MOS compatible level INTR signal drives MLA1 through a voltage divider whose ratio is chosen to guarantee V_H into MLA1 with V_{HM} into the divider, and V_L when the MOS causes the divider input to float. The 12K resistor to -12V guarantees current sinking into MLA1. Should the MOS INTR signal be OFF (V_{LM}), IG IN from the Telebus will be shunted to IG OUT on the Telebus through MLB1. If the MOS INTR signal is ON (V_{HM}), the Telebus INTR will assert (V_L) and IG IN from the Telebus will pass to the MOS IG IN to be chained to the SSI ports. Telebus IG OUT will be OFF (V_H).

2.03.6 The IN ENB signal (INENBS) is used to disable the open-collector drivers MLA2 and MLA3 such that the data is released as IN ENB turns OFF.

2.04 FS-4 (Transmit Data Interface)

2.04.1 General - Functional Block FS-4 depicts the Data/Address and control bus into the MOS send ports. The output SSI signal biasing provides the necessary input signal to the SSI signal transformers located off card.

2.04.2 The 2.7K series resistors operate with the 6.8K resistors on FS-2 to form the required voltage division for driving the Telebus.

2.04.3 The three resistors for the SSI Out signaling form the line matching (100 ohm through a 5:1 signal transformer) with the 2.4K and a voltage divider with the 3.9K resistors to ground causing a 5V p-p signal to the transformer when the MOS circuitry closes to V_{HM} .

2.05 FS-5 (Receive Data Interface)

2.05.1 General - Functional Block FS-5 depicts the Data/Address and Control Bus into the MOS receive ports. The quad-comparator (MLD9) and CMOS counter (MLC13) in conjunction with the MOS circuitry provides the necessary input for the receive SSI signalling from the SSI signal transformers located off card.

2.05.2 The 2.7K series resistors operate with the 6.8K resistors on FS-2 to form the required voltage division for driving the Telebus.

2.05.3 The receive SSI signal from the transformer differentially drives the quad-comparator (biased for hysteresis) which presents a 12V signal to the CMOS counter which, in its parallel mode and clocked with the 896 CLK, drives the MOS receiver with a synchronized MOS level signal.

2.06 FS-6 (Clock Input and Option Logic)

2.06.1 General - Functional Block FS-6 depicts the I/O Select, INENB and INIT signalling into the MOS circuitry. The 896 CLK provides the high frequency (896KHz) clock necessary for the asynchronous SSI receiver, while the 112 CLK provides the clock (112KHz) to drive the diphas SSI transmitter. The Mag Tape options and chip select options are shown driving the ports.

2.06.2 The chip select options (CS3 and CS4) in conjunction with the hard wired CS1 and CS2 provide the identity of the SSI port.

Port	Corresponding	
	D/A	<u>4</u> <u>5</u>
A	0	0
B	1	0
C	0	1
D	1	1

2.07 FS-7 (Interrupt Logic Interface and Vector Option)

2.07.1 General - Functional Block FS-7 shows the power connections to the MOS circuitry, the interrupt signal configuration and the loopback signal paths.

2.07.2 Power (V_{SS} and $-V_{DD}$) feed the MOS circuitry as shown.

2.07.3 The VBOPT signal is converted to MOS compatible voltage by the two stage amplifier Q1-Q2 to feed the MOS circuitry thereby determining the sense of the most significant bit of the vector. The INTR signal is common to all ports. IG IN is daisy chained throughout the ports establishing the following priority:

Priority	Port
High	A Send
	B Send
	C Send
	D Send
Low	A Receive
	B Receive
	C Receive
	D Receive

2.07.4 When conditioned by the control to operate loopback, pin 24 of the receive port asserts causing the serial data to appear on pin 24 of the send port. The SSI Out is held mark (28 KHz square) and the SSI IN is blinded.

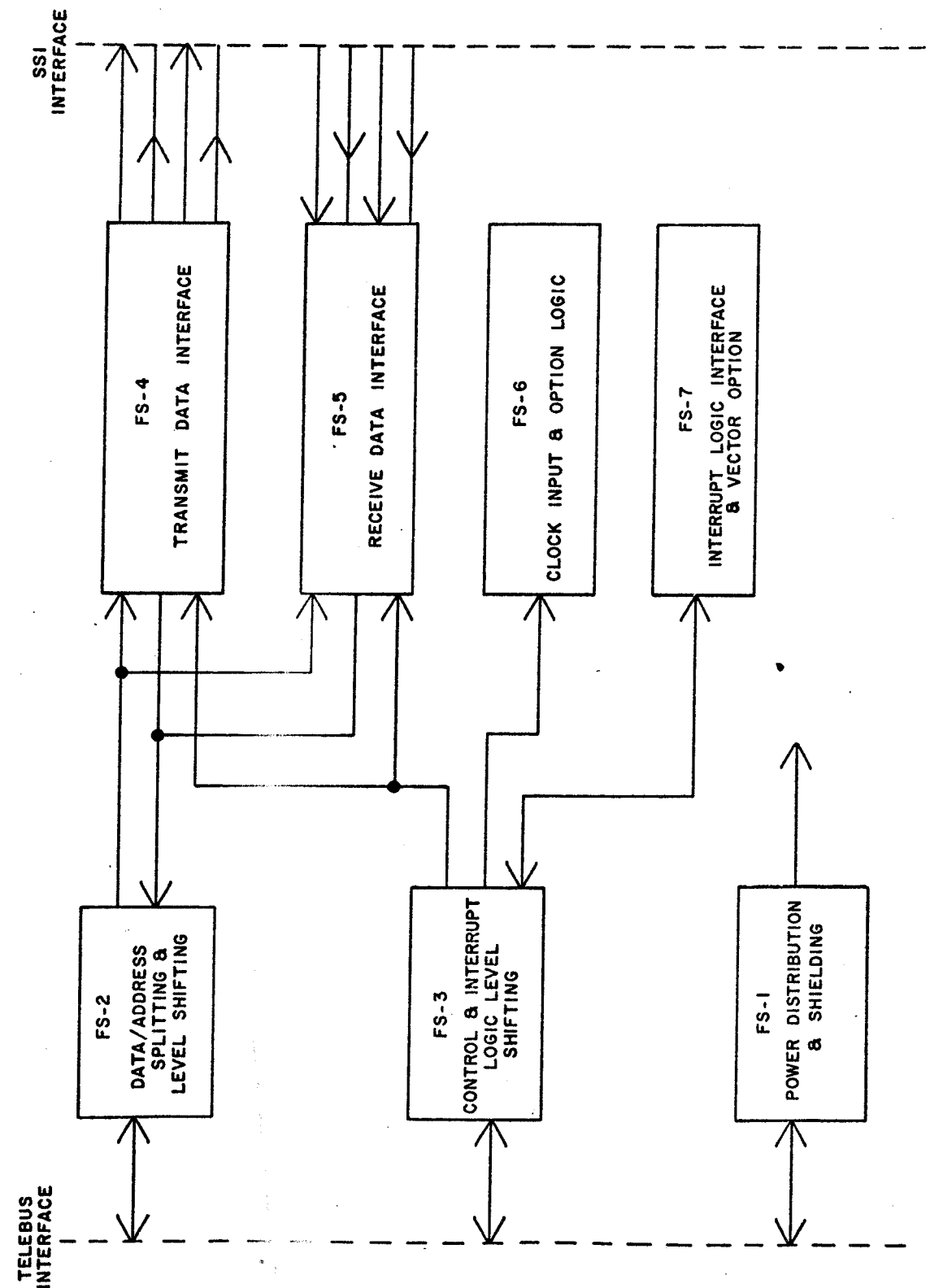


FIGURE 1

SHEET INDEX AND ISSUE CONTROL

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Sheet 1

CIRCUIT DESCRIPTION OF THE 410411 AND 410412
COMMUNICATION INTERFACE UNIT CARD ASSEMBLIES
(CIU/DIU/PIT/SID)

[illegible]

APPROVALS			ENG. DAB	DSGNR.	DRN.	
PROJ. SUPV.	PROJ. DIR.	MFG.REL. COMPL.	DATE 3/12/76	S-NUMBER		
			R & D FILE NO. 6-167-172AA	E-NUMBER		4411CD

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SHEET INDEX AND ISSUE CONTROL

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Sheet 2

CIRCUIT DESCRIPTION OF THE 410411 AND 410412
COMMUNICATION INTERFACE UNIT CARD ASSEMBLIES
(CIU/DIU/PIT/SID)

[illegible]

APPROVALS			ENG. DAB	DSGMR.	DRN.	
PROJ. SUPV. L. C. 6/29/76	PROJ. DIR. R. J. 6/29/76	MFG. REL. COMPL.	DATE 3/12/76	S-NUMBER		
			R&D FILE NO. 6-167.172AA	E-NUMBER		4411CD

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CIRCUIT DESCRIPTION OF THE 410411 AND 410412
COMMUNICATION INTERFACE UNIT CARD ASSEMBLIES
(CIU/DIU/PIT/SID)

SECTION I - USER INFORMATION

1. PURPOSE OF THE CIRCUIT

1.1 The 410411 Card Assembly contains the electronics for a Communication Interface Unit (CIU), a Programmable Interval Timer (PIT) and a Station Identification Device (SID). These devices are I/O devices for the 40C400 Controller and therefore conform to the "Telebus" input and output signalling requirements.

1.1.1 The CIU interfaces a 40C400 Controller to a data set operating in either a character and bit synchronous, character and bit asynchronous or character asynchronous, bit synchronous mode (isochronous). In synchronous and isochronous operation baud rates up to 9600 Baud are accommodated, while compatibility with a wide variety of speeds is provided in the asynchronous mode (Sec. 3.1.1).

1.1.2 The PIT provides a means of generating two independent and program-variable time delays when the device is used in a 40C400 Controller. Time delays from 0.57 ms to 75 sec may be programmed.

1.1.3 The SID provides 8 bytes of field-alterable, non-volatile read only data storage to be addressed by 40C400 operating programs. The data storage is provided by eight, eight position switches on the card assemblies.

1.2 In addition to containing the same three I/O devices as the 410411 Card, the 410412 Card Assembly contains a Dialer Interface Unit (DIU).

1.2.1 The DIU provides the 40C400 Controller with automatic dialing capability in switched network operation. Compatibility with both the 801C Data Auxiliary Set and the 851A1 Terminal Auxiliary Unit ("Integrated" Auto-Dialer used with 251A1 Terminal Data Unit) is provided.

2. FUNCTIONAL DESCRIPTION

2.1 Functional Description of the CIU (Refer to Figure 1)

To interface the 40C400 controller to a data set, the CIU converts data and control information from the line discipline and TTL signal levels of the Telebus to an EIA-RS-232C compatible interface. The exchange of information is accomplished by the operating program in the controller reading or writing data into registers located on the CIU card assembly.

2.1 (Continued)

The parallel to serial conversion of the data to be transmitted is performed by the Transmit Buffer. This register indicates it's empty/not empty state by a bit in the Status Register (see below) and is double-buffered to allow the operating program a full character time for its servicing. An interrupt occurs when the Transmit Buffer is empty (if enabled by the corresponding interrupt enable bit in Control Register 3).

The Receive Buffer similarly performs the serial to parallel conversion of incoming data characters. When a new character has been assembled, a bit is set in the Status Register and an interrupt is generated if the corresponding interrupt enable bit in Control Register 1 has been set. Double buffering of the received data allows the operating program a full character time to service this interrupt.

Send and receive baud rates are the same and are determined by a clock from the data set in synchronous and isochronous operation. In the asynchronous mode, a crystal oscillator and switches on the card assemblies select the two baud rates. The operating program can then switch between these two selected baud rates.

The Status Register is interrogated by the operating program for all status information from the CIU. Included in this information is the parity of the assembled character and the state of various data set leads. Several internal states of the CIU are also reflected in the bits of this register.

Writing into Control Register 1 allows the program to control several data set leads directly and set or clear certain internal control states of the CIU. Testing of the CIU or CIU/data set combination from the Telebus interface by an operating program is facilitated by providing two loopback modes initiated by bits in Control Register 1.

Registers 2 and 3 provide the capability of program control for various CIU features. Synchronous, asynchronous or isochronous operation, the character frame (5, 6, 7 or 8 bits per character) and additional test leads are controlled by Register 2. Control Register 3 provides the additional interrupt enable for Transmit Buffer empty and controls several other internal CIU states.

2.2 Functional Description of the PIT (Refer to Figure 2)

The variable time interval produced by each of the two timers (A and B) is generated by two presetable modulo 256 counters. These counters are connected in the count-down mode and, after being preset with a value via program control, signify expiration of the time interval when they hit the "all zeros" state. Expiration of the time interval causes the device "DONE" flag to be set. This flag generates an interrupt if the corresponding "INTR ENABLE" flag for that timer has been set by the operating program. Both of these flags are component bits of a 4 bit status register for each timer. Each status register is addressable with the proper device address. Clock

2.2 (Continued)

pulses for the two modulo 256 counters are derived by dividing the master system clock (896 KHz) with a frequency divider. This divider consists of 18 binary counting stages with output taps at stages 9, 14 and 18 generating clock signals with periods of .571 ms, 18.28 ms and 293 ms respectively. Three ranges of timing intervals are possible by providing for connection of the modulo 256 counters to one of the three prescale frequencies. Two "RANGE SELECT" bits in the status register of each timer allow selection of the prescale frequency under program control.

2.3 Functional Description of the SID

The 8 bytes of field programmable data storage are provided by 8 dual-in-line 8 position switch packages. Each switch position programs one of the 64 bits of storage. When a SID device address is properly decoded, the contents of 8 switch positions is selected and applied to the Telebus drivers to make up a byte of information.

2.4 Functional Description of the DIU (Refer to Figure 3)

To interface the 40C400 controller to an Automatic Calling Unit, the DIU converts data and control information from the line discipline and TTL signal levels of the Telebus to EIA-RS-232C compatible levels. The exchange of information is accomplished by the operating program in the controller reading the Status Register or writing data into the Control Register. The DIU is capable of generating one interrupt vector. When enabled, this interrupt is generated when the Present Next Digit lead from the ACU changes from OFF to ON.

Seven of the Control Register bits drive the digit and call control leads to the ACU directly, while the eighth bit is an interrupt enable. Three of the bits in the Status Register reflect the state of three call control leads from the ACU, while the remaining four bits control bits 3-6 of the generated interrupt vector and must be properly initialized by the program. Both the Control and Status Registers are READ/WRITE to facilitate testing.

FIGURE 1
CIU BLOCK DIAGRAM

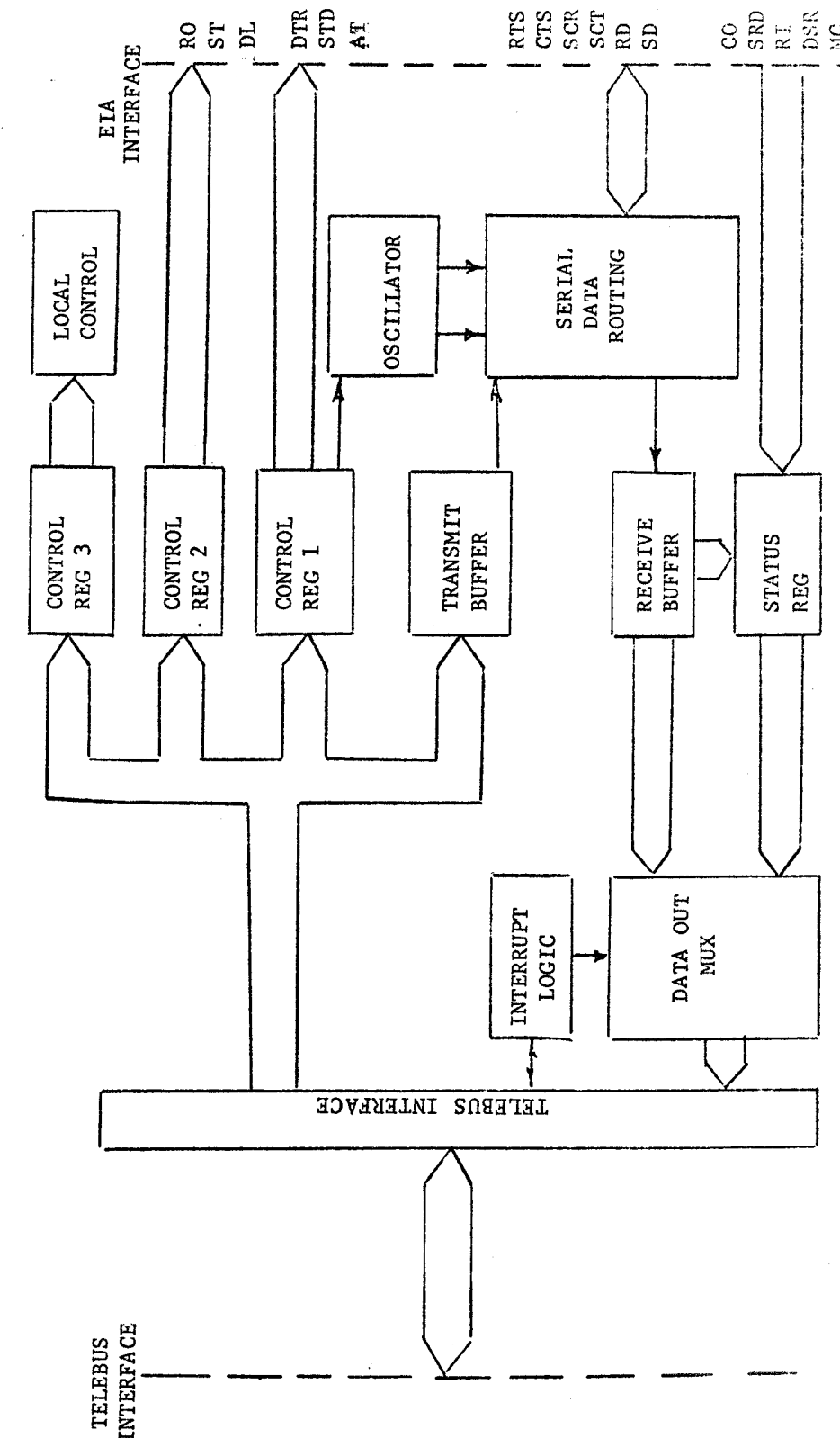


FIGURE 2
PIT BLOCK DIAGRAM

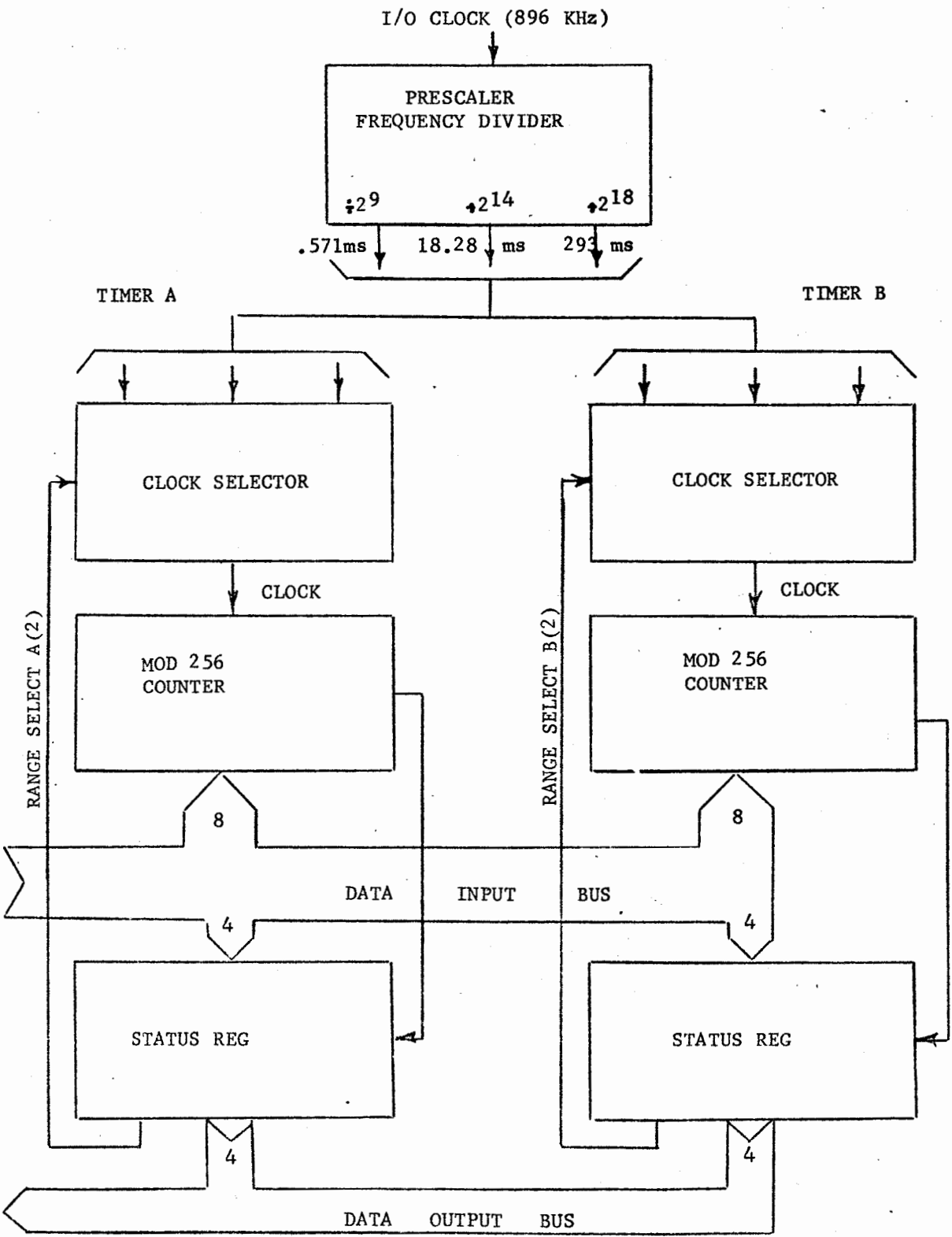
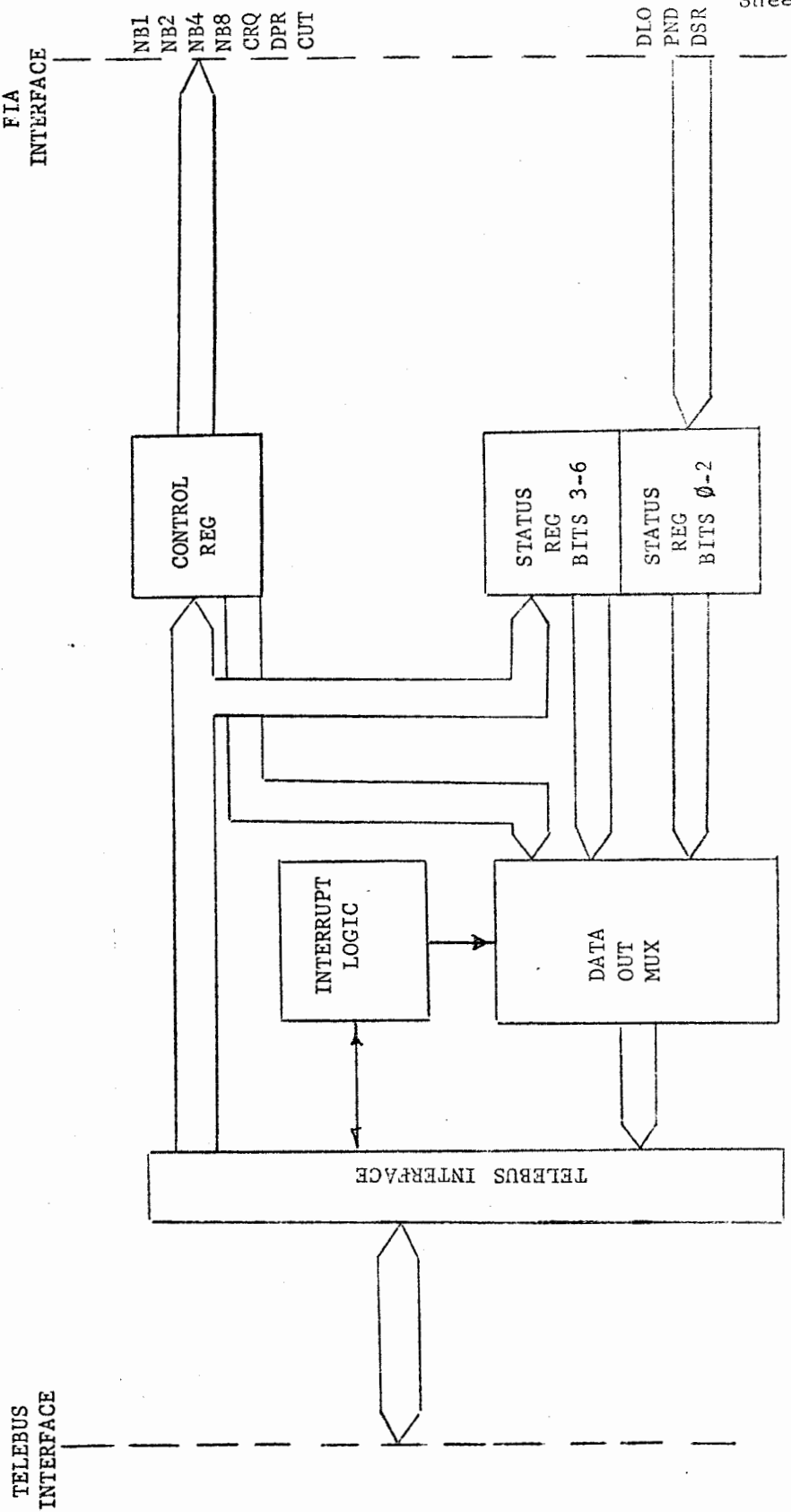


FIGURE 3
DIU BLOCK DIAGRAM



3. FEATURES

3.1 Summary of features provided by the CIU.

FEATURE

COMMENT

1. Interface to data set is EIA-RS-232C Compatible.
2. Synchronous (ASCII or EBCDIC), asynchronous or isochronous operation. Program Control
3. Compatibility with 251A1 Terminal Data Unit (Integrated Modem)
4. Synchronous/isochronous data rates up to 9600 baud.
5. Asynchronous data rates up to 3600 baud. Refer to Sec. 3.1.1.
6. Asynchronous/Isochronous character length of 5, 6, 7, 8 bits - synchronous 8-bit operation only. Program Control
7. Half Duplex/Full Duplex Operation Program Control
8. One or two STOP bits per character in asynchronous or isochronous operation. Program Control
9. Program interrupt on receive character available, receive carrier change and on transmit buffer empty. Program Control of Interrupt Enable
10. Double buffered Receive and Transmit Buffer.
11. Parity check and overrun bits provided.
12. "Sync stuffing" in transmitted data and "sync stripping" of received data. Program Control of Enable or Disable
13. Various test modes to allow the operating program to determine if the CIU card, data set, channel or far-end data set is failing. Program Control; Refer to Sec. 3.1.2.
14. Line break detection (16 bits of SPACE line) and line break generation. Program Control
15. Strap Carrier Detect ON and Modem Check OFF for compatibility with data sets not provided with these leads. Switch Options.

3.1.1 Asynchronous Baud Rates - CIU

Two baud rates are selected on the CIU card assemblies by means of switches SPA21-SW2 to SW8. The actual operating baud rate is then selected under program control from these two frequencies by Bit 7, Control Register 1.

SPEED 1 BAUD RATE TABLE (BIT 7 = 1)

SPA21-SW6	SPA21-SW7	SPA21-SW8	SPA21-SW5	Baud Rate Speed 1
OFF	OFF	OFF	X	50
ON	OFF	OFF	X	75
OFF	ON	OFF	X	100
ON	ON	OFF	X	110
OFF	OFF	ON	X	150
ON	OFF	ON	X	300
OFF	ON	ON	X	450
ON	ON	ON	X	600

X = Don't Care.

SPEED 2 BAUD RATE TABLE (BIT 7 = 0)

SPA21-SW4	SPA21-SW3	SPA21-SW2	SPA21-SW5	Baud Rate Speed 2
OFF	OFF	OFF	OFF	300
ON	OFF	OFF	OFF	450
OFF	ON	OFF	OFF	600
ON	ON	OFF	OFF	900
OFF	OFF	ON	OFF	1200
ON	OFF	ON	OFF	1800
OFF	ON	ON	OFF	2400
ON	ON	ON	OFF	3600
OFF	OFF	OFF	ON	50
ON	OFF	OFF	ON	75
OFF	ON	OFF	ON	100
ON	ON	OFF	ON	110
OFF	OFF	ON	ON	150
ON	OFF	ON	ON	300
OFF	ON	ON	ON	450
ON	ON	ON	ON	600

3.1.2 Test Modes - CIU

Several test modes are provided on the CIU card assemblies to facilitate troubleshooting a communications system.

3.1.2.1 Loopback Test (Refer to Figure 4)

When the loopback bit in Control Register 1 is set by the program, serial data from the CIU Transmit Buffer is looped back to the serial input of the Receive Buffer. The CIU then isolates itself from the associated data set and can thus be tested by the operating program independently of the data set or communications channel.

In asynchronous operation the loopback baud rate is identical to the on-line operating baud rate. In the synchronous and isochronous modes, the loopback baud rate is determined by switches SPA21-SW2 to SW5.

SPA21-SW4	SPA21-SW3	SPA21-SW2	SPA21-SW5	Loopback Baud Rate
OFF	OFF	OFF	OFF	4800
ON	OFF	OFF	OFF	7200
OFF	ON	OFF	OFF	9600
ON	ON	OFF	OFF	14400
OFF	OFF	ON	OFF	19200
ON	OFF	ON	OFF	28800
OFF	ON	ON	OFF	38400
ON	ON	ON	OFF	57600
OFF	OFF	OFF	ON	800
ON	OFF	OFF	ON	1200
OFF	ON	OFF	ON	1600
ON	ON	OFF	ON	1760
OFF	OFF	ON	ON	2400
ON	OFF	ON	ON	4800
OFF	ON	ON	ON	7200
ON	ON	ON	ON	9600

3.1.2.2 Analog Test (Refer to Figure 4)

Setting the Analog Test bit in Control Register 1 activates the Analog Test lead to the associated data set. When equipped with this feature, the data set then loops the output of the modulator to the input of the demodulator and isolates itself from the communications channel. The CIU/Data Set pair can then be tested by the operating program independently of the communications channel.

3.1.2.3 Digital Loop Test (4 wire private line test - Refer to Figure 5)

When the Digital Loop bit in Control Register 2 is set, the Digital Loop lead to the associated modem is activated by the CIU. When equipped with this feature, the data set then acts as a regenerator to the communications channel while ignoring information on the Receive and Transmit data leads from the CIU. The data set and channel can then be tested by a far end terminal in all 4 wire private line arrangements.

3.1.2.4 Two Wire Private Line Test

In 2 wire private line arrangements, the Digital Loop Test cannot be performed since a separate send and receive data path is not available on the communications channel. The following test is performed by data sets equipped with this feature using the CIU/MODEM interface leads.

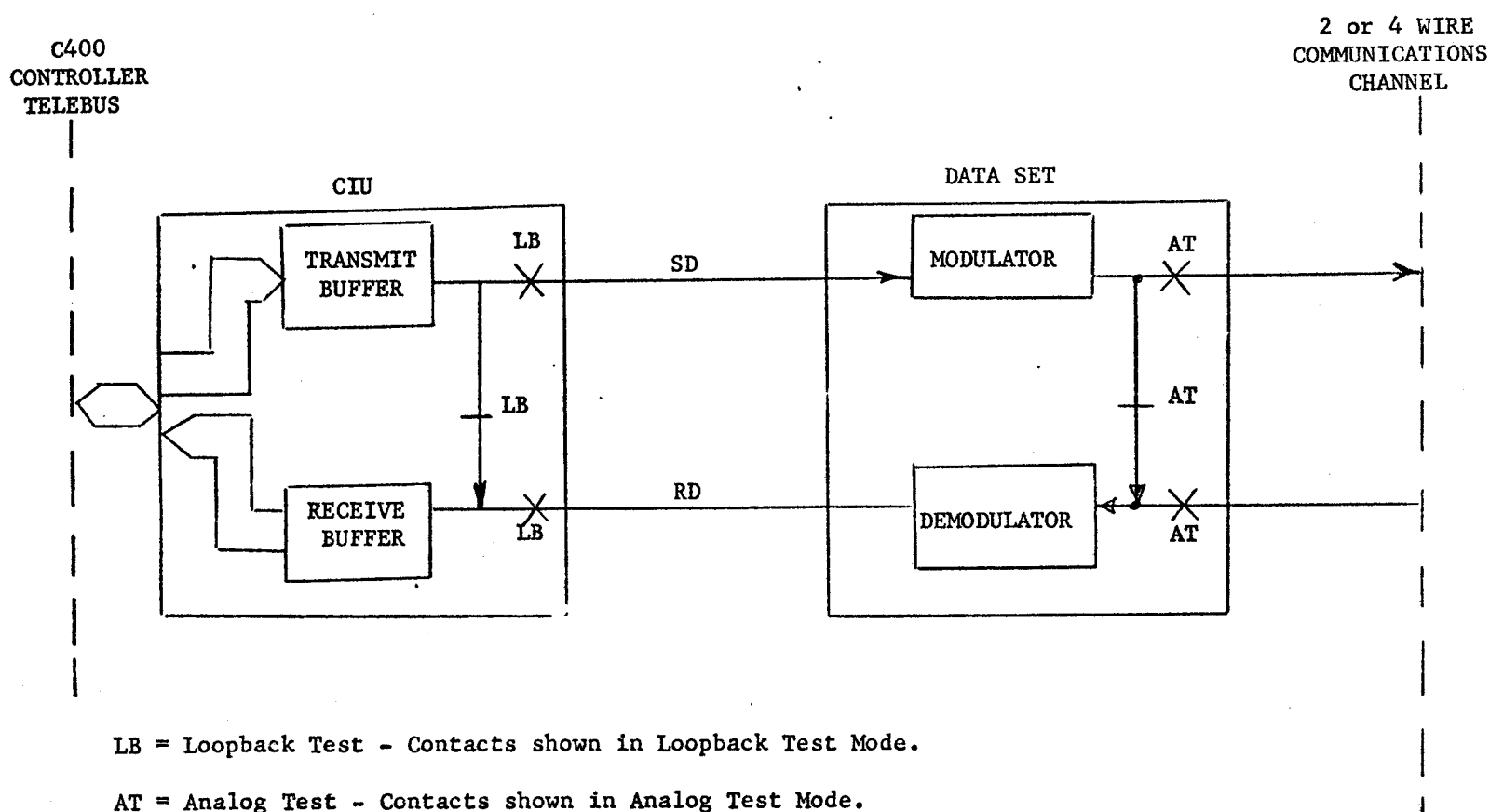
1. Self Test - This lead activates a test word generator in the data set.
2. Receive Only - When the Receive Only lead is OFF and the Self Test lead is ON, the output of the test word generator is sent by the data set to the communications channel.

When the Receive Only and Self Test leads are both ON, the data set compares the incoming test word to its locally generated test word and gives a GOOD/NO GOOD indication on the Modem Check lead.

3. Modem Check - This lead is turned ON by the data set when an error is detected in the Self Test Mode. The operating program can monitor this lead and use the information to drive a light on a control panel.

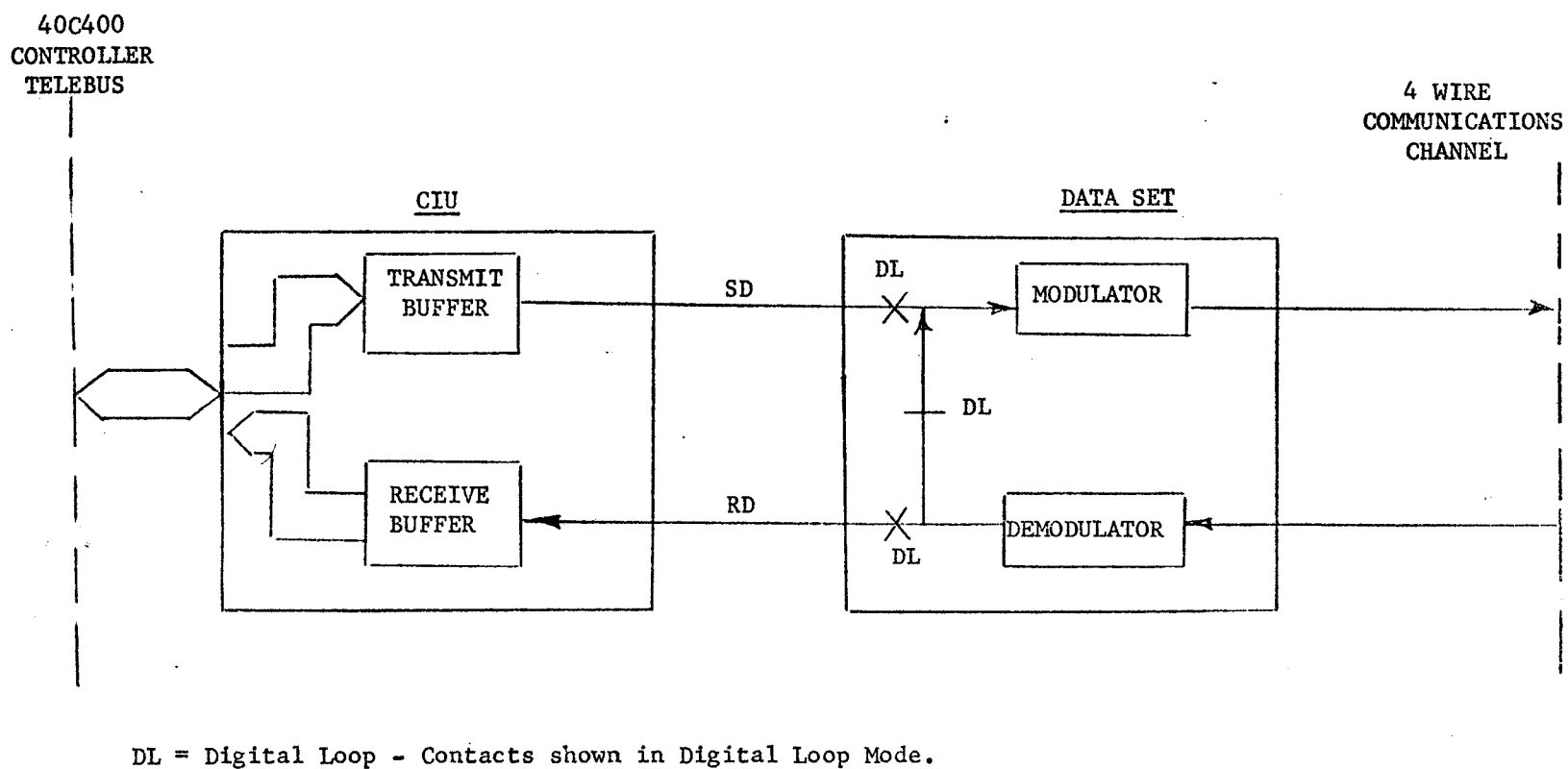
The near and far end data sets and the communications channel can then be checked independently of the terminal in a 2 wire private line arrangement.

FIGURE 4
LOOPBACK AND ANALOG TEST



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FIGURE 5
DIGITAL LOOP



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3.2 Summary of Features Provided by the PIT

The PIT provides two independent and program variable time delays from 0.571 ms to 75 sec. Independent interrupts (with associated interrupt enables) occur when the timers have completed their counts.

Timer Ranges and Accuracy

Each of the timers of the PIT can be used in any one of three different timing ranges. Each range offers a specific timer accuracy as follows:

Range No.	Timing Range (ms)	Accuracy (ms)
1	.571 - 145.6	+571, -0
2	18.28 - 4661	+18.28, -0
3	293 - 74715	+293, -0

Whenever the desired time interval can be generated with either of two available ranges, the lower range should be chosen to insure maximum accuracy.

3.3 Summary of Features Provided by the DIU:

FEATURE

1. Interface to ACU is electrically compatible with the EIA-RS-232C standard.
2. Compatible with 801C and 851A1 Terminal Auxiliary Unit.
3. Program interrupt (with associated interrupt enable) when the PND lead from the ACU changes from OFF to ON.
4. DIU Status and Control Registers are READ/WRITE to facilitate testing.

4. PROGRAMMING INFORMATION

4.1 Summary of CIU/DIU/PIT/SID Addressing and Switch Programming

Although the Telebus has a 16 bit data-address bus, only the lower byte of this 16 bit word is used for addressing. The CIU and DIU share an 8-word address block with address bits A4-A7 programmed by switches on the card assembly. The PIT and SID share two adjacent address blocks and have address bits A5-A7 programmed by switches. Since separate switches are provided for the CIU/DIU and the PIT/SID pair, there need be no relationship between the address block assigned the CIU/DIU and the two blocks assigned the PIT/SID.

To provide additional addressing capability, a DEVICE A ENABLE and DEVICE B ENABLE leads are supplied on the Telebus. Both the CIU/DIU and the PIT/SID are activated for address decoding by a DEVICE A ENABLE only.

4.1 (Continued)

By convention, bits 3 to 6 of all interrupt vectors are identical to bits 4 to 7 of the associated address block. These interrupt vector bits are thus determined by the device address. However, since the CIU and DIU require the operating program to initially write bits 3 to 6 of the interrupt vector into the proper bits of a control register, the programmer may choose not to follow this convention.

This choice is not available with the PIT. Address bits A5-A7 uniquely define interrupt vector bits IV₄ - IV₆.

4.1.1 Summary of Addresses - CIU/DIU

REGISTER	ADDRESS D/A IN 0-7	INTERRUPT VECTOR
Receive Buffer (CIU)	A7A6A5A4 0000	0IV ₆ IV ₅ IV ₄ IV ₃ 000
Control Reg (DIU)	0010	-
Status Reg (CIU)	0100	-
Status Reg (DIU)	0110	0IV ₆ IV ₅ IV ₄ IV ₃ 010
Transmit Buffer (CIU)	1000	0IV ₆ IV ₅ IV ₄ IV ₃ 100
Control Reg 1 (CIU)	1010	-
Control Reg 2 (CIU)	1100	-
Control Reg 3 (CIU)	1110	-

4.1.2 CIU/DIU Switch Programming

Switch programming of operational and loopback test baud rates is described in Section 3.1.

Switch positions are ordered from top to bottom of the switch package assembly with position 1 being at the top when the card is in the upright position. Closing of the switch results in an ON state whereas opening it is an OFF.

SPB12 Switch	Function
SW1	Address Bit A7 } ON programs a Address Bit A6 } logical '0' and Address Bit A5 } OFF programs a Address Bit A4 } logical '1'.
SW2	
SW3	
SW4	
SW8	Close at all times (Factory test switch isolates BAUD CLK from load when OPEN).

SPA21 Switch	Function
SW1	CLOSE to force a continuous Carrier Detect ON state (CLOSE when the data set does not have a Carrier Detect lead)
SW9	OPEN when the data set does not have a Modem Check lead.

4.1.3 Summary of Addresses - PIT/SID

	REGISTER	ADDRESS D/A IN 0-7	INTERRUPT VECTOR
SID	CELL 1	A ₇ A ₆ A ₅ 00000	
	CELL 2	00010	
	CELL 3	00100	
	CELL 4	00110	
	CELL 5	01000	
	CELL 6	01010	
	CELL 7	01100	
	CELL 8	01110	
PIT	TIMER A STATUS	10000	0IV ₆ IV ₅ IV ₄ 1000
	TIMER A DATA	10010	
	TIMER B STATUS	10100	0IV ₆ IV ₅ IV ₄ 1010
	TIMER B DATA	10110	

4.1.4 PIT/SID Switch Programming

SPB12 SWITCH	ADDRESS BITS PROGRAMMED	INTERRUPT VECTOR BITS PROGRAMMED
SW 5	A ₅	IV ₄
SW 6	A ₆	IV ₅
SW 7	A ₇	IV ₆

Switch positions are ordered from top to bottom of the switch package with position 1 being at the top when the card is in the upright position. Closing the switch (ON) programs a logical '0' while opening it programs a logical '1'.

4.2 Synchronous Communication Interface Unit

The Synchronous Communication Interface Unit provides the interface between the 40C400 controller and a data set operating in a character and bit synchronous mode. An 8 bit character consisting of either seven ASCII or EBCDIC information bits and a parity bit is used. Character synchronization of received data and SYN character insertion (into transmitted data) or SYN character "stripping" (received data) is performed by the CIU under program control. Loss of character synchronism is detected by the operating program (two contiguous DELETE characters for example) and is communicated to the CIU by means of the New Sync bit of Control Register 1.

Odd Parity ASCII or EBCDIC SYNC characters are detected and transmitted (when SYNC STUFFING) by the CIU. Even parity SYNC characters are considered data characters.

4.2 (Continued)

Two interrupt vectors with corresponding interrupt enable flags are provided. One interrupt is generated when a character has been received or when the state of the Carrier Detect lead from the data set changes. A different interrupt vector is sent when the Transmit Buffer changes from FULL to EMPTY.

To unburden the program, automatic control of the "Request to Send" lead (to the modem) by the CIU is provided. This lead is activated by the CIU for the duration of transmission of data or SYN characters.

4.2.1 Status Register - (READ ONLY)

ADDRESS A₇A₆A₅A₄0100

The bits of the Status Register are READ ONLY and are set and cleared by the CIU. Initialization will clear these bits.

BIT	DESCRIPTION
0	Receive Character Available - This bit is set by the CIU when the Receive Buffer contains an assembled character. An interrupt request is generated by the CIU at this time if the Receive Character Available bit had not previously been set and if the Interrupt Enable bit (bit 0, Control Register 1) is set. This bit is cleared by the CIU when the Receive Buffer is read.
1	Character Parity - This bit reflects the parity of the assembled character contained in the Receive Buffer and is updated by the CIU whenever the Receive Character Available bit is set. A "one" indicates "even" character parity and a "zero" indicates "odd" character parity. This bit is cleared by the CIU when the Receive Buffer is read.
2	Overrun/Modem Check - The meaning of this bit is determined by the state of bit 7, Control Register 2 (Modem Self Test). A) Overrun - (Bit 7, Control Register 2 Cleared) This bit is set by the CIU when two or more successive characters have been transferred into the Receive Buffer without an intervening sampling of the buffer. It indicates at least one character has been lost. This bit is cleared when the Receive Buffer is read. B) Modem Check - (Bit 7, Control Register 2 set) This bit is used in the modem SELF TEST mode. When the bit is set, an associated "Modem Check" lamp (external to the 40C400 controller) should be lit to give a visual indication of the progress of the modem SELF TEST.

4.2.1 (Continued)

BIT	DESCRIPTION
3	In Sync - This bit is set by the CIU when two consecutive SYN characters have been detected. Synchronism is then established and the Receive Character Available bit is <u>subsequently</u> set for every assembled character.
	This bit is cleared by the CIU when the New Sync bit in Control Register 1 is set by the program.
4	Transmit Buffer Available - This bit is set by the CIU when the Data Set Ready lead from the modem is ON and the Transmit Buffer is empty. An interrupt request is generated at this time if the Interrupt Enable bit (bit 7, Control Register 3) is set. Transmit Buffer Available is reset by the CIU when the Transmit Buffer is loaded with a character by the program.
5	Carrier - This bit reflects the conditions of the Carrier Detect lead from the modem. A "one" indicates a Carrier ON state.
	When the state of this bit changes, the same interrupt request as for receive character available is generated if the Interrupt Enable bit (bit 0, Control Register 1) is set.
6	Ring - This bit reflects the condition of the Ring lead from the modem. A "one" indicates a Ring ON state.
7	Not used.

4.2.2 Receive Buffer - (READ ONLY)

ADDRESS A₇A₆A₅A₄0000

The bits of the Receive Buffer are READ ONLY and are updated by the CIU when a new character has been assembled. In 5, 6 and 7 level operation, the unused high order bits of the Receive Buffer are '0' (SPACE) when read.

<u>BII</u>	<u>DESCRIPTION</u>
0-7	Receive Data Bits - Data Bits 1-8 (MARK is a "1", SPACE is a "0")

4.2.3 Transmit Buffer - (WRITE ONLY)

ADDRESS A₇A₆A₅A₄1000

The bits of the Transmit Buffer are WRITE ONLY and are set and cleared by the program when a new character is to be transmitted. In 5, 6 and 7 level operation, the unused high order bits of the data written into the Transmit Buffer must be '0' (SPACE).

<u>BIT</u>	<u>DESCRIPTION</u>
0-7	Transmit Data Leads - Data Bits 1-8 (MARK is a "1", SPACE is "0")

4.2.4 Control Register 1 - (WRITE ONLY)

ADDRESS A7A6A5A41010

The bits of Control Register 1 are WRITE ONLY and are set and cleared by the program.

Initialization will clear these bits.

<u>BIT</u>	<u>DESCRIPTION</u>
0	Interrupt Enable RCA - When set, this bit permits an interrupt by the CIU when the Receive Character Available bit is set or when the Carrier bit changes.
1	Transmit Sync - When this bit is set, SYN characters (either ASCII or EBCDIC) are automatically generated by the CIU to prevent idle intervals between transmitted characters. At the beginning of a "Request to Send"/"Clear to Send" handshaking sequence with the modem, setting this bit causes "Request to Send" (to the modem) to be activated but does not immediately result in the transmission of SYN characters. This "Sync Stuffing" does not begin until the first character has been loaded into the Transmit Buffer by the program.
2	Data Terminal Ready - When set, this bit provides the Data Terminal Ready Signal to the modem.
3	Loopback - When this bit is set, serial data from the transmitter output is sent to the receiver input of the CIU. The CIU is blinded to the Receive Data lead from the modem while the Transmit Data and Request to Send leads to the modem are held at MARK and OFF respectively.

4.2.4 (Continued)

<u>BIT</u>	<u>DESCRIPTION</u>
4	Analog Test - When set, this bit activates the Analog Test lead to the modem. If provided with this feature, the modem will then perform an analog loopback of transmitted data to the receiver input. The modem must activate all the appropriate control leads (Clear to Send, Data Set Ready, Carrier Detect) for proper data transfer to occur.
5	Program must clear this bit (not used in synchronous system).
6	Program must clear this bit (not used in synchronous system).
7	New Sync - This bit is set by the program to cause the CIU to drop character synchronization. The New Sync bit is reset by the CIU when this action has been performed.

4.2.5 Control Register 2 - (WRITE ONLY)

ADDRESS A7A6A5A41100

Initialization will clear these bits.

<u>BIT</u>	<u>DESCRIPTION</u>
0	This bit must be set for synchronous operation.
1	This bit is cleared for ASCII and set for EBCDIC operation.
2	This bit must be cleared for synchronous operation (Programs 8 bit characters).
3	This bit must be cleared for synchronous operation (Programs 8 bit characters).
4	This bit must be cleared for synchronous operation (Programs no stop pulse).
5	Digital Loop - When set, this bit activates the Digital Loop lead to the modem.
6	Receive Only - When set, this bit activates the Receive Only lead to the modem.
7	Self Test - When set, this bit activates the Self Test lead to the modem.

4.2.6 Control Register 3 - (WRITE ONLY)

ADDRESS A7A6A5A41110

Initialization will clear these bits.

<u>BIT</u>	<u>DESCRIPTION</u>
0	Half Duplex - When set, this bit disables the receive logic when the CIU is transmitting characters.
1	Request to Send - When set, this bit activates the Request to Send lead to the modem. Setting this bit is not required for data transmission. Loading a character into the Transmit Buffer will also initiate a Request to Send for the time interval required to transmit that character.
2	Strip Sync - When this bit is set, the CIU will purge SYN characters (ASCII or EBCDIC) from received data.
3-6	Interrupt Vector - The program must initially write bits 3 through 6 of the interrupt vector that is to be generated by the CIU into these bit positions respectively.
7	Interrupt Enable TBA - When set, this bit allows an interrupt by the CIU when the Transmit Buffer becomes available.

4.3 Asynchronous/Isochronous Communication Interface Unit

The Asynchronous Communication Interface Unit provides the interface between the 40C400 Controller and a modem operating in a character and bit asynchronous or a character asynchronous, bit synchronous mode (isochronous). Character lengths of 5, 6, 7 or 8 bits with one or two stop bits are accommodated. Operating baud rates up to 9600 baud are accepted in the isochronous mode while a selection of asynchronous baud rates is available (sec 3.1.1).

Two interrupt vectors with corresponding interrupt enable flags are provided. One interrupt is generated when a character has been received or when the state of the Carrier Detect lead from the data set changes. A different interrupt vector is sent when the Transmit Buffer changes from FULL to EMPTY.

To unburden the program, automatic control of the "Request to Send" lead (to the modem) by the CIU is provided. This lead is activated by the CIU for the duration of transmission of data characters.

4.3.1 Status Register - (READ ONLY)

ADDRESS A7A6A5A40100

The bits of the Status Register are READ ONLY and are set and cleared by the CIU. Initialization will clear these bits.

BIT	DESCRIPTION
0	Receive Character Available - This bit is set by the CIU when the Receive Buffer contains an assembled character. An interrupt request is generated by the CIU at this time if the Receive Character Available bit had not previously been set and if the Interrupt Enable bit (bit 0, Control Register 1) is set. This bit is cleared by the CIU when the Receive Buffer is read.
1	Character Parity - This bit reflects the parity of the assembled character contained in the Receive Buffer and is updated by the CIU whenever the Receive Character Available bit is set. A "one" indicates "even" character parity and a "zero" indicates "odd" parity. This bit is cleared by the CIU when the Receive Buffer is read.
2	Overflow/Modem Check - The meaning of this bit is determined by the state of bit 7, Control Register 2 (Modem Self Test). A) Overflow - (Bit 7, Control Register 2 cleared) This bit is set by the CIU when two or more successive characters have been transferred into the Receive Buffer without an intervening sampling of the buffer. It is an indication that one or more characters have been lost. This bit is cleared when the Receive Buffer is read. B) Modem Check - (Bit 7, Control Register 2 set) This bit is used in the model SELF TEST mode. When the bit is set, an associated "Modem Check" lamp (external to the 40000 Controller) should be lit to give a visual indication of the progress of the modem SELF TEST.
3	Framing Error - This bit is set by the CIU when a receive character does not have a valid (i.e., MARKING) STOP bit. This bit is cleared when the Receive Buffer is read.
4	Transmit Buffer Available - This bit is set by the CIU when the Data Set Ready lead from the modem is ON and the Transmit Buffer is empty. An interrupt request is generated at this time if the Interrupt Enable bit (bit 7, Control Register 3) is set. Transmit Buffer Available is reset by the CIU when the Transmit Buffer is loaded with a character by the program.

4.3.1 (Continued)

BIT	DESCRIPTION
5	Carrier - This bit reflects the condition of the Carrier Detect lead from the modem. A "one" indicates a Carrier ON state. When the state of this bit changes, the same interrupt request as for receive character available is generated if the Interrupt Enable bit (bit 0, Control Register 1) is set.
6	Ring/Receive Break - This bit is set when the Ring lead from the modem is ON or when 16 consecutive bits of SPACING receive line (line break) are detected.
7	Supervisory Receive Data - This bit reflects the state of the Supervisory Receive Data lead from suitable modems. When this lead from the modem is ON, the bit is set to a "one".

4.3.2 Receive Buffer - (READ ONLY)

ADDRESS A7A6A5A40000

The bits of the Receive Buffer are READ ONLY and are updated by the CIU when a new character has been assembled. In 5, 6 and 7 level operation, the unused high order bits of the Receive Buffer are '0' (SPACE) when read.

BIT	DESCRIPTION
0-7	Receive Data Bits - Data Bits 1-8 (MARK is a "1", SPACE is a "0")

4.3.3 Transmit Buffer - (WRITE ONLY)

ADDRESS A7A6A5A41000

The bits of the Transmit Buffer are WRITE ONLY and are set and cleared by the program when a new character is to be transmitted. In 5, 6 and 7 level operation, the unused high order bits of the data written into the Transmit Buffer must be '0' (SPACE).

BIT	DESCRIPTION
0-7	Transmit Data Leads - Data Bits 1-8 (MARK is a "1", SPACE is a "0")

4.3.4 Control Register 1 - (WRITE ONLY)

ADDRESS A7A6A5A41010

The bits of Control Register 1 are WRITE ONLY and are set and cleared by the program. Initialization will clear these bits.

BIT	DESCRIPTION
0	Interrupt Enable RCA - When set, this bit allows an interrupt to be initiated by the CIU when the Receive Character Available bit is set or additionally, when the carrier bit changes.
1	Request to Send - When set, this bit activates the Request to Send lead to the modem, indicating that the program has data to transmit. Setting this bit is not required for data transmission. Loading a character into the Transmit Buffer will also initiate a Request to Send for the time interval required to transmit that character. This bit must be set when a SEND BREAK is generated.
2	Data Terminal Ready - When set, this bit activates the Data Terminal Ready lead to the modem.
3	Loopback - When this bit is set, serial data from the transmitter output is sent to the receiver input of the CIU. The CIU is blinded to the Receive Data lead from the modem while the Transmit Data and Request to Send leads to the modem are held at MARK and OFF respectively.
4	Analog Test - When set, this bit activates the Analog Test lead to the modem. If provided with this feature, the modem will then perform an analog loopback of transmitted data to the receiver input. The modem must activate all the appropriate control leads (Clear to Send, Data Set Ready, Carrier Detect) for proper data transfer to occur.
5	Send Break - Setting this bit forces the Transmit Data lead to the modem to go SPACING. A Request to Send is not automatically generated.
6	Supervisory Transmit Data - Provides signalling capability on the reverse channel of suitable modems. When this bit is set, the Supervisory Transmit Data lead to the modem is activated (set to ON).
7	Speed Select - <u>Isochronous Operation:</u> A speed select choice is not available since the baud rate clock is supplied by the Data Set. This bit is set to "1".

Asynchronous Operation: This bit allows the program to choose one of two switch selectable baud rates. These baud rates are described in Sec. 3.1.

4.3.5 Control Register 2 - (WRITE ONLY)

ADDRESS A7A6A5A41100

Initialization will clear these bits.

<u>BIT</u>	<u>DESCRIPTION</u>															
0	This bit must be cleared (programs asynchronous/isochronous operation).															
1	This bit must be set for isochronous and cleared for asynchronous operation.															
2-3	These bits program the character length as follows:															
<u>DESCRIPTION</u>																
	<table><tr><th><u>DATA BITS</u></th><th><u>BIT 2</u></th><th><u>BIT 3</u></th></tr><tr><td>5 bits</td><td>1</td><td>1</td></tr><tr><td>6 bits</td><td>0</td><td>1</td></tr><tr><td>7 bits</td><td>1</td><td>0</td></tr><tr><td>8 bits</td><td>0</td><td>0</td></tr></table>	<u>DATA BITS</u>	<u>BIT 2</u>	<u>BIT 3</u>	5 bits	1	1	6 bits	0	1	7 bits	1	0	8 bits	0	0
<u>DATA BITS</u>	<u>BIT 2</u>	<u>BIT 3</u>														
5 bits	1	1														
6 bits	0	1														
7 bits	1	0														
8 bits	0	0														
4	Stop Code - When this bit is set, transmitted characters with two stop bits are generated while a cleared bit results in a single stop bit. When operating with 5 bit characters (5 data bits plus start and stop bits), 1-1/2 rather than 2 stop bits are generated when this bit is set.															
5	Digital Loop - When set, this bit activates the Digital Loop lead to the modem.															
6	Receive Only - When set, this bit activates the Receive Only lead to the modem.															
7	Self Test - When set, this bit activates the SELF TEST lead to the modem.															

4.3.6 Control Register 3 - (WRITE ONLY)

ADDRESS A7A6A5A41110

Initialization will clear these bits.

BIT	DESCRIPTION
0	Half Duplex - When set, this bit disables the receive logic when the CIU is transmitting characters.

4.3.6 (Continued)

BIT	DESCRIPTION
1	Request to Send - When set, this bit activates the Request to Send lead to the modem. Setting this bit is not required for data transmission. Loading a character into the Transmit Buffer will also initiate a Request to Send for the time interval required to transmit that character.
2	This bit must be cleared (not used in asynchronous/isochronous operation).
3-6	Interrupt Vector - The program must initially write bits 3 through 6 of the interrupt vector that is to be generated by the CIU into these bit positions respectively.
7	Interrupt Enable TBA - When set, this bit allows an interrupt by the CIU when the Transmit Buffer becomes available.

4.4 Programmable Interval Timer (PIT)

The program communicates with and controls the PIT by means of two registers in each of the timers.

4.4.1 Status Register

Each of the timers has a Status Register which is loaded from the program. Initialization clears these bits.

BIT	DESCRIPTION
0	DONE FLAG (Read Only) - Timing interval has expired. An interrupt with the proper vector is generated if the INTR ENABLE flag has previously been set. This bit is automatically cleared whenever a new status or data word is written, or when the interrupt it generates has been granted.
1	INTR ENABLE (Read/Write) - Permits the DONE flag to generate an interrupt when set. This bit is automatically cleared upon initialization.
2,3	TIMER RANGE SELECT bits (Read/Write) - Combination of these bits select the timer ranges as follows:

Bit Combination		Range	Range
Bit 3	Bit 2	No.	(Milliseconds)
0	0	Timer in OFF State	
0	1	1	.571 - 145.6
1	0	2	18.28 - 4661
1	1	3	293 - 74715

4.4.1 (Continued)

BIT	DESCRIPTION
2,3	(Continued) The timer range select bits are automatically cleared when the programmed interval expires. This places the timer in the OFF state. The timing operation is started (the timer starts running) as soon as the range select bits are loaded with a non-zero value from the program. These bits are also cleared automatically upon initialization. Either timer may be stopped at any time by loading zeros into these two bits via program control.
4,5,6,7	These bits of the Status Register are not used; they will be zeros when read.

4.4.2 Data Register

Each of the two timers on the PIT also has an 8-bit Data Register which may be loaded from the user program. To specify a given timeout the register is loaded with an unsigned 8-bit number in the range of 1 to 377 (octal). The time interval that will be generated for any given value of the Data Register depends on the selection of the range (via the range control bits) and is calculated as follows:

Range	Time Interval (Milliseconds)
1	.571 x n + .571, -0
2	18.28 x n + 18.28, -0
3	293 x n + 293, -0

In the above table n is the 8-bit value in the Data Register. The Data Register is write-only and will generate all zeros when read by the program.

4.5 Station Identification Device (SID)

The 8 bytes of SID information are programmed by setting 64 switches. The switches are arranged as 8 dual-in-line switch packages each with 8 switch positions. The following table relates the switch positions and the switch package locations on the circuit board to the corresponding byte and bit numbers of the SID.

4.5 (Continued)

SID BYTE NO.	BIT NO.							
	0	1	2	3	4	5	6	7
	0	SPB1 Position 1	SPB2 Position 1	SPB3 Position 1	SPB4 Position 1	SPB5 Position 1	SPB6 Position 1	SPB7 Position 1
	1	SPB1 Position 2	SPB2 Position 2	SPB3 Position 2	SPB4 Position 2	SPB5 Position 2	SPB6 Position 2	SPB7 Position 2
	2	SPB 1 Position 3	SPB2 Position 3	SPB3 Position 3	SPB4 Position 3	SPB5 Position 3	SPB6 Position 3	SPB7 Position 3
	3	SPB1 Position 4	SPB2 Position 4	SPB3 Position 4	SPB4 Position 4	SPB5 Position 4	SPB6 Position 4	SPB7 Position 4
	4	SPB1 Position 5	SPB2 Position 5	SPB3 Position 5	SPB4 Position 5	SPB5 Position 5	SPB6 Position 5	SPB7 Position 5
	5	SPB1 Position 6	SPB2 Position 6	SPB3 Position 6	SPB4 Position 6	SPB5 Position 6	SPB6 Position 6	SPB7 Position 6
6	SPB1 Position 7	SPB2 Position 7	SPB3 Position 7	SPB4 Position 7	SPB5 Position 7	SPB6 Position 7	SPB7 Position 7	SPB8 Position 7
7	SPB1 Position 8	SPB2 Position 8	SPB3 Position 8	SPB4 Position 8	SPB5 Position 8	SPB6 Position 8	SPB7 Position 8	SPB8 Position 8

Where the designation SPB1 represents the switch package located at board co-ordinate B1. A given switch is programmed for a logical '0' by closing it (ON) and a logical '1' by opening it (OFF).

4.6 Dialer Interface Unit (DIU)

The program communicates with and controls the DIU by means of a Control and Status Register.

4.6.1 Status Register - (Bits 0-2 READ ONLY; Bits 3-6 READ/WRITE)

Bits 3-6 are cleared on initialization.

Bits 0, 1 and 2 reflect the state of three ACU leads directly.

BIT	DESCRIPTION
0	Data Line Occupied - This bit reflects the state of the Data Line Occupied lead from the associated Auto Calling Unit (ACU). A "one" results when the ACU lead is ON, thereby indicating to the operating program that the channel is in use for calling, data or voice communications or testing. A call request at this time is ignored by the ACU.

4.6.1 (Continued)

BIT	DESCRIPTION
1	Present Next Digit - This bit reflects the state of the Present Next Digit lead from the ACU. A "one" results when the ACU's Present Next Digit lead is ON, thereby indicating to the program that the next digit of the called number may be presented to the ACU. When this bit is set to a "1", an interrupt is generated by the DIU if the interrupt enable bit (bit 7, Control Register) is set. When this bit is a "0" (Present Next Digit lead from ACU is OFF), bit 5 of the Control Register (Digit Present) is also held at a "0" by the DIU.
2	Data Set Ready - This bit reflects the state of the Data Set Ready lead from the associated modem. A "one" indicates that the Data Set Ready lead is ON and the modem has power ON and is in the Data mode. The Data Set Ready lead is also ON in the Analog Test mode.
3-6	Interrupt Vector - The program must initially write bits 3 through 6 of the interrupt vector that is to be generated by the DIU into these bit positions respectively.
7	Not used - This bit is "0" when read.

4.6.2 Control Register - (READ/WRITE)

All bits are cleared on initialization.

BIT	DESCRIPTION
0-3	Digit Leads - Bits 0 to 3 drive digit leads NB1, NB2, NB4, NB8 of the associated ACU respectively. A "one" activates the corresponding digit lead. (Other digit permutations may request "new dial tone" or be an "end of number" indication, depending on the particular Auto Calling Unit used.)

Digit To Be Dialed	NB8	NB4	NB2	NB1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

4.6.2 (Continued)

BIT DESCRIPTION

- 4 Call Request - When set, this bit activates the Call Request lead to the associated ACU. This bit must be set for the whole call originating period and must be cleared when Data Set Ready turns ON (bit 2, Status Register set "1").
- 5 Digit Present - When set, this bit activates the Digit Present lead to the associated ACU. This is an indication to the ACU that the digit leads NB1, NB2, NB3 and NB4 contain valid data. The digit leads must be valid as long as this bit is set.
- This bit is reset by the DIU when the Present Next Digit lead from the ACU turns OFF. The Digit Present bit can be set by the program only when the Present Next Digit bit (bit 1, Status Register) is set.
- 6 Calling Unit Test - On ACU's equipped with this feature, setting this bit activates the Calling Unit Test lead to the ACU, thereby activating the 2025 Hz. generator of the associated data set.
- 7 Interrupt Enable - When set, this bit allows an interrupt to occur when the Present Next Digit lead from the ACU turns ON.

4.7 CIU/Modem Interface Lead Description (Refer to Appendix A for a listing of all EIA-RS-232C leads and their equivalent designation on the 410411/410412 Card Assemblies).

Signal levels on the CIU/Modem interface are electrically compatible with the EIA-RS-232C standard. The complete list of interface leads accommodated by the CIU in synchronous, asynchronous or isochronous operation is listed below. A particular application will use only a sub-set of the leads as determined by the system and the hardware.

4.7.1 Transmitted Data

Direction: From Communication Interface Unit

Serial data from the CIU is transferred to the modem on this lead. When operating in the synchronous or isochronous mode, databit transitions will be presented in phase with the positive transitions of the timing signal (SCT) from the modem. The CIU will hold this lead in a MARK condition when no data is being transmitted.

4.7.2 Received Data

Direction: To Communication Interface Unit

Serial data from the modem is transferred to the CIU on this lead. When operating with synchronous modems (synchronous or isochronous operation) data bit transitions must be presented in phase with the positive transitions of the timing signal (SCR) from the modem. The Receive Data is clamped to a MARK condition in the CIU when the Carrier Detect lead is in the OFF state.

4.7.3 Transmitter Signal Element Timing (SCT) (Synchronous or Isochronous Mode Only)

Direction: To Communication Interface Unit

This interface lead provides the CIU with signal element timing information for the transmission of data from the CIU. This timing information should be present whenever the modem is in a POWER ON condition.

4.7.4 Receiver Signal Element Timing (SCR) (Synchronous or Isochronous Mode Only)

Direction: To Communication Interface Unit

This interface lead provides the CIU with signal element timing information for the sampling of the received data from the modem.

4.7.5 Control to Modem

Direction: From Communication Interface Unit

4.7.5.1 Data Terminal Ready - The ON condition of this lead indicates that the CIU is ready to transmit or receive data.

4.7.5.2 Request to Send - This lead is turned ON to condition the modem for data transmission.

4.7.5.3 Analog Test - The ON condition of this lead causes the modem to disconnect the transmitter and receiver from the channel and loopback the transmitter output to the receiver input. The modem must activate all the appropriate control leads (Clear to Send, Data Set Ready, Carrier Detect) for proper data transfer to occur.

4.7.5.4 Digital Loop - In modems equipped with this feature, the ON condition of the lead causes the modem to act as a regenerator to the channel while blinding itself to the Transmit Data lead (from the CIU) and holding the Receive Data lead MARKING. All appropriate Control leads (Data Carrier Detect, Clear to Send, etc.) are held off. Incoming data from the channel is then regenerated by the modem and is re-transmitted to the communications channel.

4.7.5.5 Self Test - In modems equipped with this feature, the ON condition of the lead causes the modem to enter the SELF TEST mode. The modem then executes TEST 2 in the 201C Technical Reference. (Used in 2 wire private line systems only.)

4.7.5.6 Receive Only - When in the SELF TEST mode, the ON condition of this lead causes the modem to act as a receiver. (Used in 2 wire private line systems only.)

4.7.5.7 Supervisory Transmit Data - This lead is used to modulate the Supervisory Transmit Data Channel of suitable modems.

4.7.6 Control from Modem

Direction: To Communication Interface Unit

4.7.6.1 Data Set Ready - This lead reflects the status of the modem. When ON, this lead indicates that the modem is powered and not in talk, test, (except Analog Test), or dial mode. This lead must be ON in the Analog Test mode.

4.7.6.2 Clear to Send - This lead indicates to the CIU that the modem is ready to transmit data. When ON, this lead indicates to the CIU that signals presented on the Transmitted Data lead will be sent to the communication channel. The OFF condition is an indication to the CIU that it should not transfer data across the Transmit Data lead.

4.7.6.3 Carrier Detect - When ON, this lead indicates to the CIU the presence of line signals at the modem receiver. The OFF condition of this lead indicates that no signal is being received or that the received signal is unsuitable for demodulation. With this lead OFF, the CIU will blind the Received Data from the modem.

4.7.6.4 Ring Indicator - When ON, this lead indicates that a ringing signal is being received by the modem.

4.7.6.5 Modem Check - This lead is used in the SELF TEST mode of the data set to give a visual indication of the progress of the test. The ON condition of this lead causes a "Modem Check" lamp (external to the 40C400 Controller) to be lit at the terminal. (Used in 2 wire private line systems only.)

4.7.6.6 Supervisory Receive Data - This lead reflects signal conditions on the Receive Supervisory Data Channel of suitable modems.

4.8 DIU/ACU Interface Leads

Signal levels on the DIU/ACU interface are electrically compatible with the EIA-RS-232C Standard.

4.8.1 Leads to the Auto-Calling-Unit (ACU) -
(Refer to a description of these leads in Section 4.6.2)

NB1 - Digit Lead
NB2 - Digit Lead
NB4 - Digit Lead
NB8 - Digit Lead
CRQ - Call Request
DPR - Digit Present
CUT - Calling Unit Test

4.8.2 Leads from the Auto-Calling-Unit (ACU) -
(Refer to a description of these leads in Section 4.6.1)

DLO - Data Line Occupied
PND - Present Next Digit

SECTION II - DETAILED DESCRIPTION

1. GENERAL

1.1 The voltages required by the card assembly have the following tolerances:

<u>Voltage</u>	<u>Voltage Range</u>
+12V	+10.8V to +13.2V
+ 5V	+ 4.5V to + 5.5V
-12V	-10.8V to -13.2V

Additionally, three identical voltages are generated on the card assembly as drain supply voltages for the three MOS packages.

<u>Voltage</u>	<u>Voltage Range</u>
-6.2V	-5.58V to -6.82V

1.2 Since an integrated circuit package may have a multitude of logic circuits shown separately on the schematic and since they all have the same ML designation, the following convention is used in the circuit description to give a unique designation to each circuit.

MLA6-(8)

ML - Refers to multilogic
A6 - Refers to Circuit Package A6, a unique designation which describes the location of that package on the card assembly.
(8) - Refers to the pin number of the output of the circuit.

Although they contain many complex functions, the MOS integrated circuit packages are shown in the schematic as single blocks.

1.3 Logic Symbols - Positive logic symbols are used in the associated schematic (4411SD).

1.4 Signal Designation - Signal leads are labeled with a title descriptive of the function of the signal. A line may or may not be drawn over this title, indicating that the signal is in the LOW or HIGH state respectively when the state described by the title of the signal is present.

2. BLOCK DIAGRAM

2.1 A general description with associated block diagram of the CIU, DIU, PIT and SID is contained in Section I, sub-section 2.

3. DETAILED DESCRIPTION

3.1 FS-1 Telebus Interface (Refer to TC-1, Telebus Signalling)

3.1.1 General - Functional block FS-1 interfaces the card to the Telebus, decodes the address of the CIU/DIU to provide a SELECT signal, and decodes the Telebus controls $\overline{C_0}$, $\overline{C_1}$, $\overline{C_2}$ to supply READ, LA (load address) and WR (write) commands to the MOS integrated circuit packages.

3.1.2 Data/Address Lines and Bus Transceivers

All data, control and address information into the card and data, status and interrupt vector information from the card appears on the eight wires, $\overline{D/A0} - \overline{D/A7}$. A HIGH on this bus is a logic '0' or SPACE while a LOW is a logic '1' or MARK. The bus drivers of MLA10 and MLA11 are open collector drivers with resistor pull-ups provided externally to the card.

Bus transceivers MLA10, MLA11 normally function as receivers so that whatever data appears on the $\overline{OUT0} - \overline{OUT7}$ leads at this time is not significant. Only when inputs 7 and 9 of MLA10 (and MLA11) are both LOW is this data gated out to the Telebus. This occurs when a READ command is decoded and either the CIU, DIU or PIT has its READ ENABLE output active (HIGH).

3.1.3 Telebus Control Decode (Refer to TC-1, Telebus Signalling)

The control leads from the Telebus are buffered and inverted by the bus receivers of MLD3 and MLD1. Control inputs $\overline{C_0}$, $\overline{C_1}$ and $\overline{C_2}$ are multiplexed to provide the following functions:

$\overline{C_2}$	$\overline{C_1}$	$\overline{C_0}$	MNEMONIC	FUNCTION
HIGH	HIGH	HIGH	NOP	No Operation
HIGH	HIGH	LOW	RDV	Read
HIGH	LOW	HIGH	LAR	Load Address
HIGH	LOW	LOW	LAD	Load Address
LOW	HIGH	HIGH	WW	Write
LOW	HIGH	LOW	WB	Write
LOW	LOW	HIGH	NOP	No Operation
LOW	LOW	LOW	NOP	No Operation

These control leads are valid when BUS ENB is LOW (approximately 560 ns for LA, WR and 1680 ns for READ).

After being gated with BUS ENB and decoded by MLD5, the READ, LA and WR signals are the real-time read, load address and write commands for the card.

3.1.4 Address Decode (CIU/DIU)

The high order four bits of the CIU/DIU address block (A4, A5, A6, A7) are encoded by switches SPB12-SW4, 3, 2 and 1 respectively. A switch closure is a logic '0' while an open switch is a logic '1'.

These four switches are compared to inputs $\overline{D/A4} - \overline{D/A7}$ from the Telebus by address comparator MLA12. This comparator is enabled when both BUS ENB ($\overline{D/A0} - \overline{D/A7}$ valid) and DEV A ENB (device falls in 'A address' group) are LOW. Note however, that the LA (load address) signal is not gated in. The SELECT signal is therefore HIGH whenever bits 4-7 of the Telebus agree with the switch programming. This active SELECT signal therefore only has significance when the LA signal is LOW simultaneously, thereby indicating that the CIU/DIU has been addressed. This SELECT signal is latched in the CIU/DIU (MLA16, MLA20 and MLA18) when the LA signal is LOW.

3.1.5 The INIT signal from the Telebus is an asynchronous power on reset of several milliseconds duration.

3.1.6 A free running 896 KHz. clock is supplied to the card assembly on the I/O clock lead. It is used as a time base for the interval timers and generates timing pulses internal to the CIU-R (MLA16).

3.2 FS-2 Clock Circuit

3.2.1 The asynchronous baud rates available in the CIU (refer to Section I, sub-section 3.1.1) are generated by division of the BAUD CLK signal in the CIU-T (MLA20). The output of oscillator MLC14 is divided by either 11 or 12 in MLC13 depending on the state of signal DIVIDE BY 11 (a HIGH indicates division by 11). This output from the CIU-T (MLA20) will indicate division by 11 at all times other than when 110 BAUD operation is selected. In the latter case, the LOW on DIVIDE BY 11 causes MLC13 to divide the output of MLC13 by 12.

3.3 FS-3 Interrupt Arbitration

3.3.1 Input MLD3-15 acts as a summing point for the interrupt requests of the CIU, DIU and PIT. Any one request causes this input to be HIGH and consequently the INTR interrupt request to the Telebus to be LOW.

Active interrupt grant in signals (INTG IN LOW) are passed directly to the INTG OUT line to the Telebus at all times other than when the card has an interrupt request pending. Input MLD4-2 is then LOW causing INTG OUT to be HIGH, thereby preventing the interrupt grant signal from propagating through the card.

When a CIU/DIU interrupt is being serviced, the INTR REQ input to MLD3-15 will typically be reset during the READ interval (i.e., when READ is LOW and the interrupt vector is being read). The DC latch formed by gates MLD4-(8) and MLD4-(11) prevents the INTG OUT signal from becoming active while the CIU/DIU interrupt is being serviced.

3.4 FS-4/FS-5 Communication Interface Unit Transmitter and Receiver (Refer to TC-2 and TC-3.)

3.4.1 General

The CIU-T (MLA20) in conjunction with the CIU-R (MLA16) and peripheral components form a Communications Interface Unit (CIU) that interfaces a 40C400 Controller to a data set. A functional description, block diagram, list of features, addresses of the registers and a detailed description of the bits of the registers is contained in Section I, sub-sections 2, 3 and 4. Described below are the details of the signal leads and the interaction of the CIU-T and CIU-R.

3.4.2 MOS Packages MLA16, MLA20

These devices are P-channel, enhancement mode MOS microelectronic assemblies that contain the receive (MLA16) and transmit (MLA20) logic of the CIU. Source and drain voltages of +5V and -6.2V and a gate voltage of -12V supply power to the packages. All output drivers conduct to +5V (when ON), with a low voltage supplied by an external pull down resistor when the driver is OFF.

3.4.3 Since the receive and transmit functions of the CIU are in different packages, not all registers and bits are present in both devices. The following summary therefore provides insight into which functions are performed in which device. (An X indicates bit is used.)

Status Register

<u>BIT</u>	<u>DESCRIPTION</u>	<u>CIU-R</u>	<u>CIU-T</u>
0	Receive Character Available	X	
1	Character Parity	X	
2	Overrun/Modem Check	X	
3	In Synch/Framing Error	X	
4	Transmit Buffer Available	X	
5	Carrier	X	
6	Ring/Receive Break	X	
7	Supervisory Receive Data	X	

Receive Buffer

<u>BIT</u>	<u>DESCRIPTION</u>	<u>CIU-R</u>	<u>CIU-T</u>
0-7	Receive Data Bits 1-8	X	

Transmit Buffer

<u>BIT</u>	<u>DESCRIPTION</u>	<u>CIU-R</u>	<u>CIU-T</u>
0-7	Transmit Data Bits 1-8		X

3.4.3 (Continued)

Control Register 1

<u>BIT</u>	<u>DESCRIPTION</u>	<u>CIU-R</u>	<u>CIU-T</u>
0	Interrupt Enable-RCA	X	
1	Request to Send/Transmit Sync		X
2	Data Terminal Ready		X
3	Loopback	X	X
4	Analog Test	X	X
5	Send Break		X
6	Supervisory Transmit Data		X
7	New Sync/Speed Select	X	X

Control Register 2

<u>BIT</u>		<u>DESCRIPTION</u>	<u>CIU-R</u>	<u>CIU-T</u>
<u>BIT 1</u>	<u>BIT 0</u>			
0	0	Asynchronous	X	X
0	1	Synchronous - ASCII	X	X
1	0	Isochronous	X	X
1	1	Synchronous - EBCDIC	X	X
<u>BIT 3</u>	<u>BIT 2</u>			
0	0	8 Bit Char Length	X	X
1	0	7 Bit Char Length	X	X
0	1	6 Bit Char Length	X	X
1	1	5 Bit Char Length	X	X
	4	1 or 2 Stop Bits		X
	5	Digital Loop		X
	6	Receive Only		X
	7	Self Test		X

Control Register 3

<u>BIT</u>	<u>DESCRIPTION</u>	<u>CIU-R</u>	<u>CIU-T</u>
0	Half Duplex	X	
1	Request to Send		X
2	Strip Sync	X	
3-6	Interrupt Vector Bits 3-6	X	
7	Interrupt Enable - TBA	X	

3.4.3 (Continued)

As can be seen from the above list, the Status Register, Receive Buffer and all bits associated with generation of interrupt vectors are contained only in the CIU-R. Therefore, although both devices are written into from the Telebus, only the CIU-R is read (data flow from CIU to Telebus).

3.4.4 Load Address, Read and Write

Address or data information from the Telebus is written into MLA16 and MLA20 on inputs D/A IN0-7 when LA or WR is LOW respectively. (A HIGH on the data lines will set a '1'.) The SELECT signal (indicating the CIU address has been decoded) and IN1, 2 and 3 are latched in the CIU-R and CIU-T when LA is LOW, thereby selecting one of the 6 registers. Data may then subsequently be written into this register on these same D/A IN0-7 leads when WR is LOW.

Immediately after the address of a CIU/DIU register has been latched in the CIU-R, it is assumed that this register is to be read (even if it is a WRITE ONLY register). The READ ENABLE CIU lead becomes active and the register data (if register is readable) is presented on the OUT0-7 leads. This data is not gated out to the Telebus by FS-1 until a READ is decoded. Note however, that the READ input to the CIU-R is not involved in reading of data from MLA16.

3.4.5 Interrupt Vectors

Interrupt requests are generated by the CIU-R (if enabled) when a data character is received, the state of the Carrier lead from the modem changes or the TBA lead (Transmit Buffer Available) changes to HIGH. The INTR REQ CIU lead is then set HIGH.

The interrupt is granted by the Telebus when INTG IN changes to HIGH. At this time, READ ENB CIU becomes active and the interrupt vector is present on data leads OUT0-7, although it is not gated out to the Telebus by FS-1 until READ is LOW. The READ input to the CIU-R resets the interrupt request after it has been granted.

INTG OUT CIU reflects the state of INTG IN at all times other than when an interrupt request is pending. In the latter case, INTG OUT CIU is held OFF so that devices (DIU, PIT) sampling this lead will not simultaneously generate an interrupt vector.

3.4.6 Speed Selection

Input BAUD CLK supplies the time base that allows the CIU-T to generate a large selection of asynchronous baud rates. Switch package SPA21 controls the baud clock divider chain in MLA20 and selects two baud rates, one of which is then chosen as the operating baud rate by bit 7, Control Register 1. (Refer to Section I, sub-section 3.1.1 for a list of these speeds.) The loopback test baud rate is similarly selected (Section I, sub-section 3.1.2).

3.4.6 (Continued)

The frequency of BAUD CLK is 921.6 KHz. for all baud rates other than 110 Baud. In the latter case, DIVIDE BY 11 is LOW causing BAUD CLK to have a frequency of .844.8 KHz.

The LOCAL CLOCK lead passes a frequency of 16 times the baud rate clock to the CIU-R in the asynchronous mode.

In synchronous or isochronous operation clocks at the baud rate frequency are supplied on the SCT and SCR leads from the data set. Loopback testing however is performed at a baud rate determined by the CIU-T. (1X clock is then present on LOCAL CLOCK).

3.4.7 Data Transmission and Reception

A HIGH TAB (Transmit Buffer Available) signal indicates that the double buffered Transmit Buffer in MLA20 is empty and can be loaded with a data character from the Telebus. Serial data characters are then sent on the SD lead at the operating baud rate when CTS is ON.

In the loopback mode, serial data is looped from the CIU-R to the CIU-T on the LOOP DATA lead while SD is held MARKING.

Similarly, serial receive data from the data set is on the RD lead and is deserialized by the CIU-R.

A visual indication of the state of the SD and RD leads is provided by light emitting diodes CR3, CR4 and CR1 and CR2 respectively.

3.4.8 Additional Drivers and Receivers to Data Set

The following leads to the data set are directly controlled by bits in Control Registers of the CIU-T.

RTS	Request to Send
DTR	Data Terminal Ready
STD	Supervisory Transmit Data (Reverse Channel)
AT	Analog Test
RO	Receive Only
DL	Digital Loop
ST	Self Test

Additionally, RTS is also ON whenever a data or SYN character is transmitted. The RTS signal is required by the CIU-R to allow blinding RD in half duplex operation when Request to Send is ON.

The following inputs to the CIU-R from the data set control bits in the Status Register of MLA16. Additionally, a switch closure of A21-1 overrides the CO input and provides a continuous carrier ON state.

CO	Carrier Detect
SRD	Supervisory Receive Data (Reverse Channel)
RI	Ring
MC	Modem Check

3.4.8 Test 1, Test 2, Outenable (T1, T2, OUT ENB)

These three inputs are provided to facilitate card testing.

When T1 is LOW and T2 is HIGH (as driven by a test set external to the card assembly), a 16X baud rate clock (on lead BAUD CLK) can be used to clock the CIU directly, bypassing the clock divide chains in MLA20.

When OUTENB is driven LOW by an external test set, all output drivers of the CIU-R are turned OFF.

3.4.9 I/O CLOCK Input (Refer to Section II, sub-section 3.1.6.)

3.5 FS-6 Dialer Interface Unit

(NOTE: The DIU is available on the 410412 Card Assembly only.)

3.5.1 General

The DIU (MLA18) with external EIA amplifiers and receivers forms a Dialer Interface Unit that interfaces a 40C400 Controller to an Automatic Calling Unit (ACU). A functional description, block diagram, list of features, addresses of the registers and detailed description of the bits of the registers is contained in Section I, sub-sections 2, 3 and 4.

3.5.2 MOS Package MLA18

This device is a P-channel, enhancement mode MOS microelectronic assembly requiring source and drain power supplies of +5V and -6.2V respectively and a gate supply voltage of -12V. All output drivers conduct to +5V (when ON) with a LOW voltage supplied by an external pull down resistor when the driver is OFF.

3.5.3 Definition of Registers and Bits

The DIU contains two registers that are used by the operating program to control the associated ACU. A detailed description of these registers is contained in Section I, sub-section 4.6.

3.5.4 Load Address, Read and Write

Loading of addresses, reading of, or writing data into the Control or Status Registers is identical to the operation of the CIU-R described in Section II, sub-section 3.4.4. The LA, WR, SELECT, READ ENB DIU, IN0-7 and OUT0-7 leads are used for this purpose. Operation differs only in that both the Control and Status Registers of the DIU are READ/WRITE.

3.5.5 Interrupt Vector

One interrupt vector is generated by the DIU (if enabled) when the Present Next Digit lead from the ACU turns ON. The INTR REQ DIU lead is then HIGH, indicating an interrupt is pending.

Two 'interrupt grant in' signals are provided on MLA18. INTG IN1 is common to all the interrupting devices (CIU-R, DIU, PIT) and, when active, freezes the interrupt status of the device. The INTG IN2 is the daisy-chained 'interrupt-grant-in' from the Telebus that passes through all interrupting devices and is intercepted by the first device on the chain that has an interrupt pending.

Generation of the vector in response to INTG IN, activation of READ ENB DIU and resetting of the serviced interrupt vector by READ is identical to the CIU-R operation (Section II, sub-section 3.4.5).

3.5.6 Operation of the DIU

A call may be originated from the operating program when the Data Line Occupied lead from the ACU is OFF. The ON condition of this lead indicates that the communication channel is in use for calling, data communication, voice communication or testing of the Data Set or ACU. When the Call Request lead to the ACU is turned ON, the Auto Calling Unit will ask for the first digit of the number to be dialed by activating the Present Next Digit lead. This causes an interrupt by the DIU (if enabled) and should result in the operating program presenting the digit and turning ON the Digit Present lead by writing into the DIU Control Register.

Successive digits are thus dialed at the rate of approximately 50 ms per digit.

At the end of the dialing sequence, the Present Next Digit lead from the ACU remains ON while the operating program waits for the Data Set Ready lead to turn ON, indicating that the call has been established.

3.5.7 Drivers and Receivers to Autocalling Unit (ACU)

The following leads to the ACU are directly controlled by bits in the Control Register.

NB1, NB2, NB4, NB8	Digit Leads
CRQ	Call Request
DPR	Digit Present
CUT	Calling Unit Test

The following leads from the ACU are directly reflected in bits of the Status Register.

DLO	Data Line Occupied
PND	Present Next Digit
DSR	Data Set Ready

3.5.8 Outenable (OUT ENB)

This input is provided to facilitate card testing. When OUT ENB is driven LOW by an external test set, all output drivers of the DIU are OFF.

3.6 FS-7 Programmable Interval Timer (PIT)

3.6.1 General

The PIT/SID (MLA14) provides two independent and program variable time delays for 400400 operating programs. A functional description, block diagram, list of features, addresses of the registers and a detailed description of the bits of the registers is contained in Section II, sub-sections 2, 3 and 4.

3.6.2 MOS Package MLA14

Similarly to the CIU-R, CIU-T and DIU devices, the PIT/SID is a P-channel enhancement mode MOS microelectronic assembly requiring +5V, -6.2V and -12V power supply voltages. All output drivers conduct to +5V (when ON) with a LOW voltage supplied by an external pull down resistor when the driver is OFF.

3.6.3 Address Decode (PIT/SID)

The high order three bits of the PIT/SID address block (A₅, A₆, and A₇) are encoded by switches SPB12-SW5, 6 and 7 respectively. A switch closure is a logic '0' while an open switch is a logic '1'. These same switches drive inputs SW5, SW6 and SW7 of MLA14 and thus directly determine bits 4, 5 and 6 respectively of the generated interrupt vector.

Address comparator MLD12 compares these switches to IN5, IN6 and IN7 when enabled by BUS ENB (IN5, IN6, IN7 valid) and by DEV A ENB (device falls in A address group). Note that the LA (load address) signal is not gated in. The SELECT signal is therefore HIGH whenever bits 5-7 of the Telebus agree with the switch programming. This active SELECT signal, however, is only of significance when LA is LOW simultaneously, thereby indicating that the PIT or SID has been addressed. This SELECT signal is latched in MLA14 when LA is LOW.

3.6.4 Load Address, Read and Write

Loading of addresses, reading of or writing data into the registers is very similar to the operation of the CIU-R described in Section II, sub-section 3.4.4. The LA, WR, SELECT, READ ENB PIT, IN0-7 and OUT0-7, leads are used for this purpose. Operation differs in the following areas:

As in the CIU-R, IN1, 2 and 3 are latched into MLA14 when $\overline{LA}$ is LOW. Additionally, inputs D/A IN3A and D/A IN4 are driven by IN3 and IN4 and stored by $\overline{LA}$. When D/A IN3 and D/A IN3A are driven by the same signal (as in the case on the 410411 and 410412 Card Assemblies), the PIT uses the lower four addresses of its assigned address block (containing 8 addresses).

3.6.4 (Continued)

Input IN4 determines if the SID or PIT has been selected.

Operation differs from the CIU-R in that 3 of the Status Register bits are READ/WRITE, one is READ ONLY, and in that the Data Register is WRITE ONLY. The READ ENB PIT signal is HIGH when either the PIT or SID has been selected.

3.6.5 Interrupt Vectors

Each of the timers in MLA14 generates an interrupt vector (if enabled) when it has completed its time-out. The INTR REQ PIT lead is then HIGH, indicating an interrupt is pending.

Two 'interrupt grant in' signals are provided on MLA14. INTG IN1 is common to all the interrupting devices (CIU-R, DIU, PIT) and freezes the interrupt status of the device when active. The INTG IN2 is the daisy-chained 'interrupt grant in' from the Telebus that passes through all interrupting devices and is intercepted by the first device on the chain that has an interrupt pending.

Generation of the vector in response to INTG IN, activation of the READ ENB PIT and resetting of the serviced interrupt vector by READ is identical to the CIU-R operation (Section II, sub-section 3.4.5).

3.6.6 Outenable Input (OUT ENB)

This input is provided to facilitate card testing. When OUT ENB is driven LOW by an external test set, all output drivers of the PIT/SID (MLA14) are OFF.

3.6.7 Outputs $\overline{A}$, $\overline{B}$, $\overline{C}$, SEL SID

These outputs are used to drive 74251 eight to one multiplexers (or equivalent) of the SID, thereby selecting one of the eight bytes of the Station Identification Device (SID) to be read by the operating program. (Refer to Section II, sub-section 3.7.)

3.7 FS-8 - Station ID (SID)

3.7.1 The 8 bytes of field programmable data storage are provided by 8 dual in-line 8 position switch packages (SPB1 - SPB8). Each switch assembly is connected to the 8 data inputs of a multiplexer package. A switch assembly-multiplier pair provides one bit of storage for all eight bytes of information.

Since the multiplexers are 'wire anded' with the outputs of the CIU-R, DIU and PIT, their outputs may be active only when the SID has been selected. This is achieved by a SEL SID signal activating the tri-state outputs of the 8 to 1 multiplexers at the proper time (when a SID address has been decoded). An OUT ENB signal (FS-7 area E5) assures that no matter what address decoding errors occur, the TTL output drivers of the multiplexers are never ON simultaneously with the MOS drivers of the CIU-R, DIU or PIT. The relationship between the select leads (A,B,C), D/A IN1, 2, 3, 4 and the particular SID byte selected is as follows:

3.7.1 (Continued)

SELECT LEADS FROM M1A14			SELECTED BYTE		D/A INPUTS WHEN LA = LOW			
C	B	A			IN4	IN3	IN2	IN1
0	0	0	Byte 1	0	0	0	0	0
0	0	1	Byte 2	0	0	0	0	1
0	1	0	Byte 3	0	0	0	1	0
0	1	1	Byte 4	0	0	0	1	1
1	0	0	Byte 5	0	0	1	0	0
1	0	1	Byte 6	0	0	1	0	1
1	1	0	Byte 7	0	0	1	1	0
1	1	1	Byte 8	0	0	1	1	1

Where 1 = HIGH voltage
0 = LOW voltage

The byte of data that has been selected by A, B and C inputs is gated out to the telebus when a READ LOW signal is present.

APPENDIX A

EIA INTERFACE CONNECTOR PIN ASSIGNMENTS (Note 2)

Pin Number
(EIA Connector-
External to Card
Assemblies)

EIA RS-232C Nomenclature

Lead Designation
(410411/410412 Card Assemblies)

1	Protective Ground (AA)
2	Transmitted Data (BA)
3	Received Data (BB)
4	Request to Send (CA)
5	Clear to Send (CB)
6	Data Set Ready (CC)
7	Signal Ground (Common Return) (AB)
8	Received Line Signal Detector (CF)
9	(Reserved for Data Set Testing)
10	(Reserved for Data Set Testing)
11	Unassigned
12	Sec. Rec'd Line Sig. Detector (SCF)
13	Sec. Clear to Send (SCB)
14	Secondary Transmitted Data (SBA)
15	Transmitter Signal Element Timing (DCE Source) (DB)
16	Secondary Received Data (SBB)
17	Receiver Signal Element Timing (DCE Source) (DD)
18	Unassigned
19	Secondary Request to Send (SCA)
20	Data Terminal Ready (CD)
21	Signal Quality Detector (CG)
22	Ring Indicator (CE)
23	Data Signal Rate Selector (DTE/DCE Source) (CH)
24	Transmit Signal Element Timing (DTE Source) (DA)
25	Unassigned
	Non EIA (Note 1)
	Non EIA (Note 1)
	Non EIA (Note 1)
	Non EIA (Note 1)
	Non EIA (Note 1)

Frame Ground (FG)
Transmitted Data (SD)
Received Data (RD)
Request to Send (RTS)
Clear to Send (CTS)
Data Set Ready (DSR)
Signal Ground (SG)
Carrier Detect (CO)
Not Used
Not Used
Supervisory Transmit Data (STD)
Supervisory Receive Data (SRD)
Not Used
Not Used
Transmitter Signal Element Timing (SCT)
Not Used
Receiver Signal Element Timing (SCR)
Not Used
Not Used
Data Terminal Ready (DTR)
Not Used
Ring Indicator (RI)
Not Used
Not Used
Not Used
Analog Test (AT)
Digital Loop (DL)
Receive Only (RO)
Self Test (ST)
Modem Check (MC)

Note 1: These leads may or may not be brought out to the EIA connector depending on the hardware in the 40C400 Controller and on the application.

Note 2: This is a typical assignment of the interface leads from the 410411/410412 card assemblies to pins on the EIA connector. Since this connection is made external to the card assembly, other lead assignments may be made to fit other applications.

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4430CD

CIRCUIT DESCRIPTION FOR
THE 410430 DISPLAY I/O LOGIC

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2	1	1	1	1	2	2	2	1	1	1	2	1	1

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APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG.REL. COMPL.
		bm

ENG.
J.G.

DSGNR.

DRN.

DATE
2-14-75

S-NUMBER

R & D FILE NO.

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4430CD

TELETYPE CORPORATION
Circuit Description

4430 CD
Sheet 2
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CIRCUIT DESCRIPTION FOR
THE 410430 DISPLAY I/O LOGIC

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DIO CIRCUIT CARD
CC430-459

SECTION I - GENERAL TECHNICAL DATA

1. General Description

1.01 The CC430-459 Card Assembly provides the interface between the C400 Controller and the Display Monitor. It performs the function of taking selected areas of the C400 Memory and converting the contents of those areas to a form suitable for display on the 40MN101 or 102 monitor. Contained on the card are the 80 bit registers called the cache, font ROMs, attribute logic, timing, control, bus interface, and video circuitry.

2. Supporting Information

2.01 See 4430 SD and 410430-459 assembly drawing for supporting information.

SECTION II - DETAILED DESCRIPTION

1. Functional Block Diagram - Figure 1

1.01 Referring to Figure 1, the timing block provides the proper signals to the horizontal and vertical sweep generators in the display monitor. It also directs the control logic to interrupt the C400 when the monitor needs new data to display. The control logic responds by interrupting the C400 and through the use of the RBT instruction transfers eighty 16-Bit words into the cache. These 80 words are split into 160 eight bit words sufficient for two text lines of display on the monitor.

1.02 Seven bits of each eight bit word are ASCII encoded and the eighth bit is used for attribute information. The seven bits are inputted to the font ROMs which convert ASCII code to dot information. The dot information is then serialized and presented to the monitor as video. Bit 8 can take on several meanings depending on the state of the attribute logic which is under program control.

2. Display Timing - Pages 4 and 5 of 4430 SD

2.01 All display timing starts with the 18.9 MHz crystal clock, MLD21. This represents the dot frequency. It is applied to MLC19, the dot counter, arranged to divide by nine to count the number of dots per character. The TC output is used to load the video serializer and the ECL latches once per character. Outputs Q1, Q2, and Q3 clock other parts of the DIO.

2.02 The divide-by-100 character counter is clocked by the dot counter at the 2.1 MHz character rate. It consists of binary counters MLA3 and MLA5 and ROM decoder MLA4 with the counter outputs applied as addresses to the ROM. The ROM decodes four functions of the character counter: Character 99, character 96, character blank, and horizontal drive. Character 99 resets the counter to zero. Character 96 clocks the scan line counter. Character blank is used to inhibit cache clocking and to blank the screen during horizontal retrace, characters 80-99. Horizontal drive is used to drive the monitor, characters 76-26. The counter outputs are also used in the cursor compare logic MLB4 and MLB9.

2.03 The scan line counter is clocked by character 96 of the character counter and is arranged to divide by fourteen, the number of scan lines per text line. It consists of binary counter MLA15 and ROM decoder MLA14 with the counter outputs applied as addresses to the ROM. The fifth address is last text line, TL24. The ROM decodes four different permutations of the scan line counter, LSL, $\overline{LSL}$, ULSL, and an enable signal. LSL and $\overline{LSL}$ are opposite polarity signals indicating the display is on the last scan line of a text line. ULSL indicates the scan line that the character underline is activated. Output 3 is an enable signal for the data multiplexers which is low only during the LSL of the last text line, TL24. Output 5 is not used at the present time but it is an enable signal for the Monolithic Memories 10K character generator. The counter's Q outputs are also sent to the font ROMs as scan line addresses. First scan line, FSL is derived from the TC output of the counter and is used as the text line clock.

2.04 The text line counter consists of MLB10, MLA10, and MLA11 and is arranged to divide by 25, the number of text lines per page. Text lines 1-24 are displayed, TL25 is used for vertical retrace and TL24 is used in the control logic. Output Q0 of the counter is called odd text line, OTEL, and is combined with TL25 for use in the control logic. TL25 is also used for the generation of the 60 Hz vertical retrace signal to the monitor, for blanking of the display during that text line, and for loading the cursor registers MLB5 and MLB7. The counter outputs are also used in the cursor compare logic MLB9.

3. Font ROMs - Page 3 of 4430 SD

3.01 The organization of the font ROMs provide some important features for the DIO. Each ROM operates independently of the others, each providing 32 symbols contained in a 9x14 dot matrix. By virtue of the wired - OR active-low outputs, removal of any of the ROMs results only in the loss of the symbols in those ROMs (the screen will blank any accessed symbol that is not on the board). Therefore, although the DIO is capable of displaying 128 symbols with four ROMs, significant cost reductions are possible if all symbols are not required for certain applications. Also, since all the scan lines of each text line are now programmable special graphic symbols can be generated which will allow continuous horizontal and vertical lines or bars as well as a new family of characters with descenders.

3.02 ASCII bits 1 through 5 are applied as common addresses to MLA17, MLA18, MLA19 and MLA20. ASCII bits 6 and 7 and their complements are used as chip enables to select one of four ROMs. The four scan line counts from MLA15 are applied as common addresses to all the ROMs. Each ROM output is wired - OR'ED to the same output on the other three ROMs and applied to the video shift register as dot information.

3.03 In operation ASCII information is presented to the ROMs at the 2.1 MHz character rate for 80 characters. The ROMs convert the ASCII into dot information for each character of that scan line. The scan counter then increments one count and the same 80 characters are presented to the ROMs. This continues for each of the 14 scan lines which make up one text line of data at which time the text line counter increments and a fresh set of ASCII is presented for the next 14 scan lines. Figure 2 illustrates the make-up of two such characters.

3.04 Significant cost reductions are possible if, in an application, lower case and control characters are not required. A strap option, ST1, is available on the board that maps any incoming lower case or control characters to the upper case and numeric ROMs respectively. This allows removal of the lower case and control character ROMs and is released as the 410434 Card Assembly. If mapping is not required, the lower case and control ROMs can simply be removed.

4. Video Circuits - Page 4 of 4430 SD

4.01 The video logic consists of the video shift register MLB18, ECL hex latch MLB20, ECL line driver MLC21, ECL EX-OR MLA21, and associated resistor packs RPB17, RPB19, and RPB21. The ECL logic operates with reduced signal swing, i.e., logic 0 = low = +3.4 volts, logic 1 = high = +4.3 volts. Resistor pack RPB17 converts the TTL logic levels to ECL logic levels.

4.02 Dot information from the font ROMs is applied to the video shift register, MLB18, at the 2.1 MHz character rate. While the last dot of the previous character is being displayed the dot information for the next character is parallel loaded into the shift register. It is then clocked out at the 18.9 MHz dot rate and appears at MLC21-13 as video. Here it is gated with character blanking information from the attribute logic and wire - OR'ED with underline information also from the attribute logic. The ECL latch MLB20 is used to insure that the attribute information is displayed over the correct dots of each character.

4.03 EX-OR gate MLA21 is used to invert all video coming from MLC21-14, if the cursor lead from MLB20-3 is high. This output is applied to the video line driver MLC21-9 where it is gated with retrace blanking and the 18.9 MHz clock from MLC20-10. This clock gating chops the video into 25NS pulses which are sent differentially over a balanced, impedance - matched transmission line to the monitor. Intensify information from MLA10-11 is applied to the junction of R17 and R18 through R13. When the intensify lead goes low sufficient current is drawn through R18 to force a logic low to MLC21-11. This has the effect of removing the 18.9 MHz clock from the gate which allows the full 53NS video pulse to be sent over the transmission line. This longer duration dot will appear brighter, though more distorted, than the surrounding characters on the monitor screen.

4.04 Half-intensity information from the attribute logic is applied through ECL latch MLB20-4 to line driver MLC21-4 where it is gated with retrace blanking and sent over the transmission line to the monitor.

5. Cursor Logic and Attribute Mode Register - Page 2 of 4430 SD

5.01 The cursor logic consists of hex registers MLB5, MLB6, MLB7, MLB8 and hex comparators MLB4 and MLB9. MLC15 is the attribute mode register.

5.02 Once each refresh during the last text line, TL24, the control logic presents a sync program interrupt to the C400. The C400 responds by sending a single 16 bit word to the DIO which is stored in registers MLB6, MLB8, and MLC15. Bits 0 through 6 represent the character position the cursor is to appear. Bits 8 through 12 represent the text line the cursor is to appear, and bits 13, 14, and 15 tell the DIO how to respond to attribute commands during that refresh. The contents of the attribute mode register are used as addresses for the attribute decoding ROM MLC16.

5.03 The contents of the cursor registers are transferred to MLB5 and MLB7 during vertical retrace. During the scanning of the next refresh the comparators MLB4 and MLB9 compare the register contents to the character and text line counts and when they coincide a cursor is generated and sent to the video logic MLB20-12.

6. Control Logic and Bus Interface - Page 5 of 4430 SD

6.01 The control logic performs the hand-shaking routine with the C400 for the transfer of data from memory to the DIO. Since the DIO requires new information from the C400 every two text lines, the timing logic informs the control logic when the data is required. The control logic responds by stepping through a sequence of events; presenting an interrupt vector, enabling the input caches to accept data, synchronizing the data with the display, and returning to an idle mode. This sequence is performed by the sequence counter MLB2, state decoder MLB1, selector MLC1, and control bus decoder MLC2.

6.02 Figure 3 is a state diagram describing the sequence that the control logic steps through. The states are numbered and correspond to the count of the sequence counter, MLB2. Transitions between states occur when the condition indicated between states is satisfied, i.e., a transition from state 7 to state 0 will occur during FSL, first scan line.

6.03 Assume that sequence counter is in state 0. The control logic will remain here until the timing logic requests new data. This request comes in the form of OTEL+VBLK, i.e., when the timing is not in an Odd Text Line or is in the Vertical BLANK interval the sequence will be started by stepping to state 1. State 1 waits for the lead INTG-IN, interrupt grant in, to go high indicating the bus is not servicing an interrupt at the present time and steps the control logic to state 2. During state 2 the control logic presents an interrupt to the C400 by taking the INTR lead low. The INTG-OUT lead is taken high to prevent other devices from interrupting, and the control logic waits for the C400 to assert the INTG-IN lead and to present the RDV code on the control leads C0, C1, and C2. At this time the interrupt vector is sent out on the bus by MLC5 as determined by vector switches 1, 2, and 3 and the control sequence steps to state 3.

6.04 During state 3 the INTR is held low while the INTG-OUT is maintained at a 1. The presence of the first RDI on the control leads will step the sequence counter to state 4. The RDI instruction will last for 80 bus cycles and as long as RDI remains on the control leads the counter will remain in state 4 and the input caches will be loaded with the data on the data/address leads of the bus. When RDI goes low the sequence counter goes to state 5, an inactive state, waiting for the timing logic to indicate that Data Blank is at a 0. At that time the sequence counter steps to state 6 and waits for Data Blank to return to a 1, at which time the counter increments to state 7. The control logic remains in state 7 until the timing logic asserts the first scan line (FSL) of the next text line, then the control logic returns to state 0.

6.05 The nucleus of the control logic is sequence counter MLB2, state decoder MLB1 and selector MLC1. Sequence counter MLB2 is a synchronous 4-bit binary counter with synchronous parallel load and clear inputs. The sequence counter is clocked by Bus Enable, twice inverted from the Telebus, and the counter is clock enabled by the output of selector MLC1. The selector receives as address inputs the outputs of the sequence counter and uses the low 3 bits, counts 0 thru 7, to select one of eight data inputs to supply at the output of the selector. The high order bit from the sequence counter is ignored allowing the state decoder to step from state 7 back to state 0.

6.06 The data inputs to selector MLC1 are the signals which, when asserted, will enable the sequence counter to increment to the next state. These signals are those shown in Figure 3 as conditions for state to state transitions. The data inputs to the selector are driven from two sources, the Telebus control leads and the display timing logic. The Telebus control leads are decoded by ROM MLC2 which drives some of the data inputs of selector MLC1. The remaining data inputs of the selector are driven by the command register, MLA2. The command register is used to synchronize the signals from the display timing logic with the sequence counter and is clocked at the Telebus frequency gated by the display clock.

6.07 State decoder MLB1 inputs the binary coded state signals from the sequence counter and outputs active low signals for counts 0 thru 7. The outputs of the state decoder are used by the various small scale gates which are involved with clock switching for the caches and negotiation with the interrupt leads.

6.08 Interface with the Telebus is accomplished by receivers MLC3, MLC9, and MLC14 plus transceiver MLC5. The data/address leads are received by MLC5, MLC9 and MLC14 which invert and output these signals to input cache shift registers MLC6, MLC8, MLC10 and MLC13, to cursor registers MLB6 and MLB8 and to attribute mode register MLC15. Receiver MLC3 inputs Telebus Control Leads C_0 , C_1 , and C_2 , Bus Enable, Initialize, and Interrupt Grant In.

6.09 Since the DIO board generates interrupt vectors only in the range 0 - 16_8 or 400_8 - 416_8 , the DIO needs to drive only four of the data address leads, D/A2, D/A3, D/A8, and D/A1. The first three of these are switch selectable by DIP switch SPC4, while D/A1 is driven by TL24* from the command latch, MLA2, and used to differentiate between a data interrupt vector and the sync vector. An interrupt vector is allowed onto the Telebus by the two active low enables on MLC5. Bus Enable drives one enable to coordinate the vector with the Telebus timing and the fifth output of control bus decoder MLC2 uses the other enable to synchronize the vector with the other interrupt proceedings. Vector switch programming information is found on the 4430 SD sheet 1.

7. Cache and Cache Control - Page 2 and 5 of 4430 SD

7.01 Following the exchange of interrupt grant and vector, the control logic is ready to load the data from the Telebus. Data is stored as eighty 16 bit words in the input cache shift registers MLC6, MLC8, MLC10, and MLC13. Each 16 bit word is comprised of two 8 bit characters for the display. If the displayed characters are counted from 0 thru 79, the even numbered characters are read from the Telebus as the low order byte of each word and are stored in caches MLC6 and MLC10. Odd numbered characters comprise the high byte of each word and are stored in caches MLC8 and MLC13. Since the data is available from the input caches two characters at a time, this data is multiplexed by MLC7 and MLC12 and presented to display caches MLB12 and MLB13.

7.02 Clocking, loading and recirculation of the input and display caches is controlled through MLA7, MLA8 and portions of MLA6, MLA9 and MLA12. The display caches are clocked by the 2.1 MHz character clock gated with Data Blank, this clock provided at MLA12-3. Loading of the display caches is accomplished during the last scan line (LSL) by removing the recirculate signal to the display caches and allowing the new line of data from the multiplexers to fill the display caches while the previous line is being used for display of that last scan line. The input caches are clocked at various times by three different clocks. When the input caches are being loaded from the Telebus, the control logic activates gates from MLA6, MLA7, and MLA8 to enable the input caches to be clocked by Bus Enable. After the new data has been loaded and before it is transferred to the display caches, the input caches are recirculated at the display character rate due to the dynamic nature of the caches. This is also under direction of the control logic along with gates from MLA6, MLA7 and MLA8. Finally, when a text line of data is being transferred from the input caches to the display caches, the two-to-one multiplexing from input to display necessitates that the input caches be clocked at one half of the display character rate. This is accomplished by applying one cycle of the display character clock to two of the input caches and then applying the next cycle to the other pair of input caches. Gates from MLA7 and MLA9 are used to perform this switching.

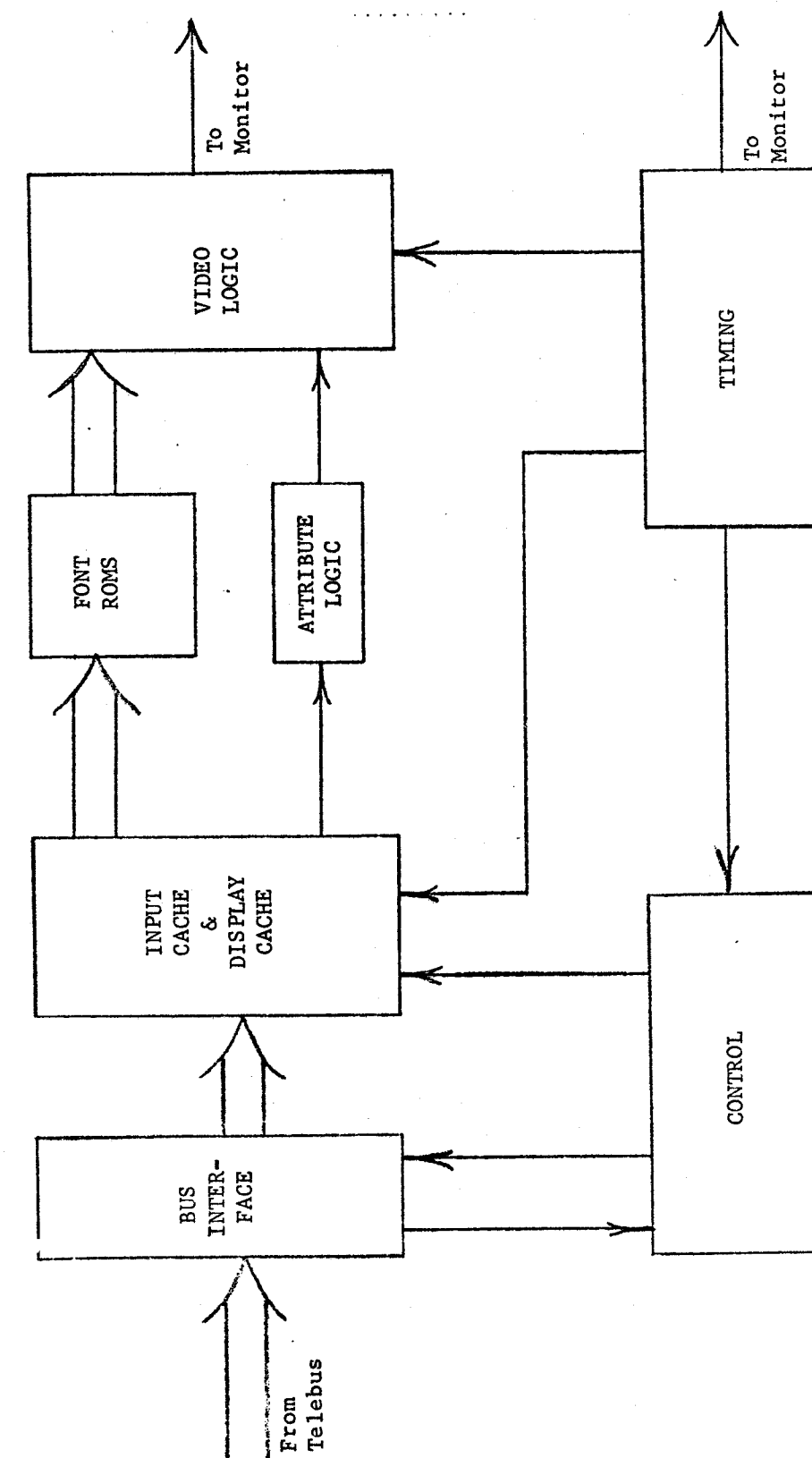
7.03 Between the inputs caches and display caches the multiplexers serve to unpack the 16 bit words to two 8 bit characters. Selection of the correct multiplexer input is performed by a signal at one half the frequency of the display character clock plus a control signal decoded from the scan line counter. Enabling of the multiplexers is used to prevent the display caches from seeing unwanted data during the last scan line of text line 24.

7.04 Data out of the display caches is strobed into latches MLB14 and one half of MLB15. This guarantees sufficient set up time for the addressing of the font ROMs.

8. Attribute Logic - Page 3 of 4430 SD

8.01 Display attributes such as half-intensity, underline, intensify and blank are controlled by the attribute logic. The attribute logic in turn is controlled by the contents of the attribute mode register MLC15 which is loaded once each refresh with D/A bits 13, 14, and 15. The attribute decoding ROM MLC16 decodes these three bits into 1 of 8 modes in which the DIO is to operate for that refresh. ASCII bits 3, 4, and 8 are processed by 1/2 MLC16, MLC17, and MLC18 before being presented to the decoding ROM. Figure 4 describes how the DIO operates for each of the eight modes.

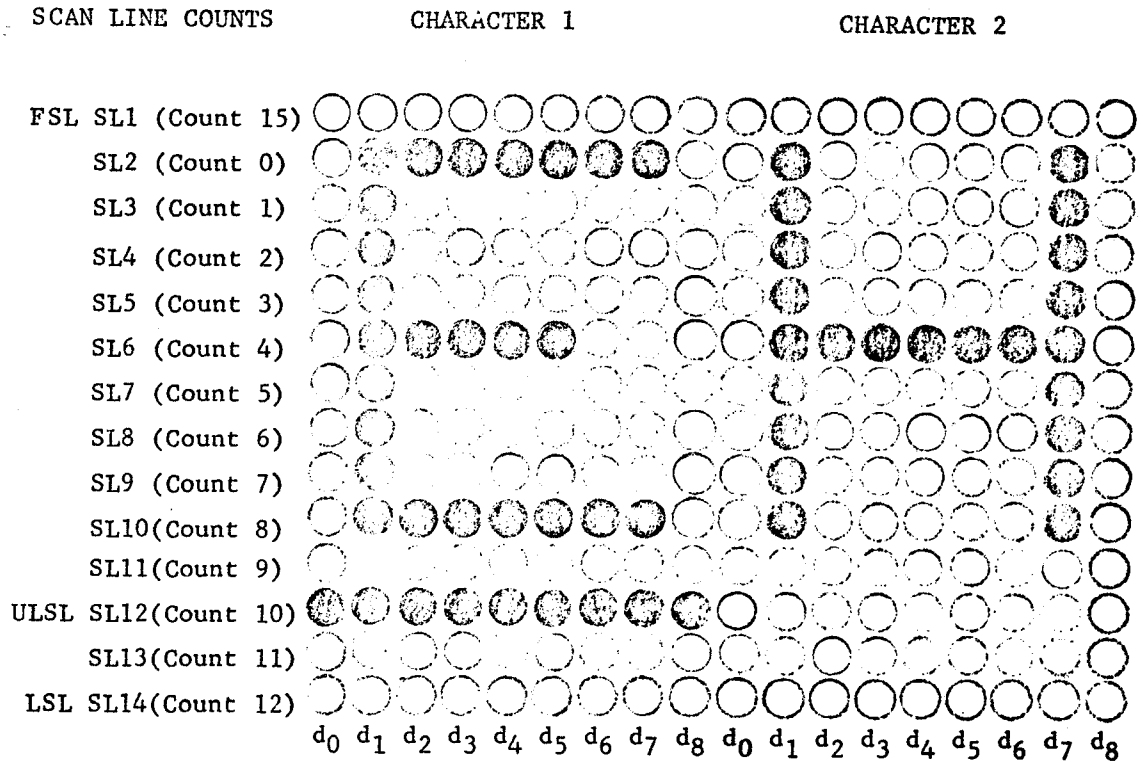
8.02 During the LSL of every text line when data is being transferred to the display caches, ASCII bits 3, 4, and 8 are loaded into attribute cache, MLC17, via latch MLC16. The attribute cache is clocked at the same time the display cache is clocked to keep the attribute bits in sync with the ASCII bits. Register MLC18 provides the same time delay to the attribute bits as register MLC14 provides for the ASCII bits. The attribute bits 3, 4, and 8 are then applied to the decoding ROM MLC16 which outputs the appropriate attribute and sends it directly to the video logic.



DIO FUNCTIONAL BLOCK DIAGRAM

FIGURE 1

CHARACTER GENERATION



Presented in parallel
to the video shift register
during D₈ of the previous
character.

CHARACTER GENERATION

FIGURE 2

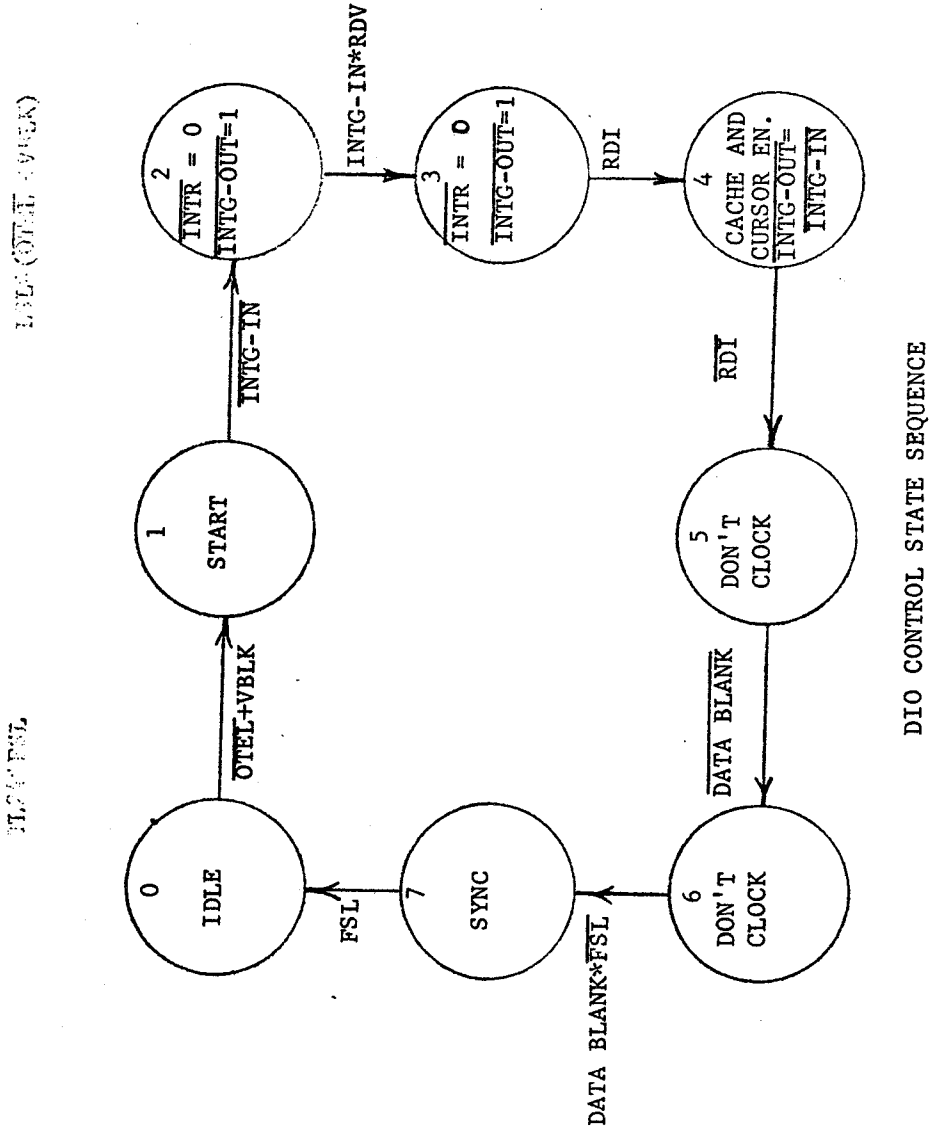


FIGURE 3

DI/O-8 ATTRIBUTE OPERATION

MODE D/A Bits 13, 14, & 15 of Cursor word loaded into parameter register once each refresh				ATTRIBUTE CHARACTER (DI/O-8 examines ASCII Bits 3, 4 and 8 of each character)			DESCRIPTION OF DISPLAY
D/A13	D/A14	D/A15		Bit 3	Bit 4	Bit 8	
#1	0	0	0	X	X	X	All characters displayed at normal intensity.
#2	0	0	1	X	X	0	Character displayed at normal intensity.
				X	X	1	This character underlined.
#3	0	1	0	X	X	0	Character displayed at normal intensity.
				X	X	1	This character displayed at half intensity.
#4	0	1	1	X	X	0	Character displayed at normal intensity.
				X	X	1	This character blanked.
#5	1	0	0	X	X	0	Char. displayed at normal intensity
				X	X	1	This character intensified.
#6	1	0	1 (IBM 3270 Equiv.)	0	0	1	Sets up a normal field. This char. blanked.
				0	1	1	Sets up an intensified field. This character blanked.
				1	0	1	Sets up a normal field. This char. blanked.
				1	1	1	Sets up a blank field. This char. blanked.
				X	X	0	Displays the field that was set up.

FIGURE 4

DI/O-8 ATTRIBUTE OPERATION

MODE D/A Bits 13, 14, & 15 of Cursor word loaded into parameter register once each refresh				ATTRIBUTE CHARACTER (DI/O-8 examines ASCII Bits 3, 4 and 8 of each character)			DESCRIPTION OF DISPLAY
D/A13	D/A14	D/A15		Bit 3	Bit 4	Bit 8	
#7				0	0	1	Sets up a normal field. This char. blanked.
				0	1	1	Sets up a half-intensity field. This character blanked.
				1	0	1	Sets up a normal field. This char. blanked.
				1	1	1	Sets up a blank field. This char. blanked.
				X	X	0	Displays the field that was set up.
#8				0	0	1	Sets up a normal field. This char. blanked.
				0	1	1	Sets up a half intensity field. This character blanked.
				1	0	1	Sets up an underlined field. This character blanked.
				1	1	1	Sets up an intensified field. This character blanked.
				X	X	0	Displays the field that was set up.

X = Don't Care

Note: Modes 2,3,4, and 5 are character attribute modes in that only ASCII Bit 8 is examined. These are similar to the Model 40 DL291 as opposed to the IBM 3270 field attribute modes.

FIGURE 4

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CIRCUIT DESCRIPTION FOR THE
410464 AND 410465 8K/4K READ/WRITE MEMORY CIRCUIT CARD ASSEMBLY

SECTION I - USER INFORMATION

1. General

1.1 The 410464 and 410465 RAM circuit cards are 8K and 4K read/write (R/W) random access memory (RAM) assemblies respectively, which provide a means of storing information. The memory is composed of semiconductor elements in which the information is internally stored on a capacitor. It is therefore volatile, losing its stored information whenever memory power is removed.

1.2 The storage capability is either 8192 words (8K) or a depopulated 4096 words (4K) of 16 bits in width. Data may be written in either a word mode or a byte (half-word) mode under control of the Instruction Execution Logic (IXL). All read operations are done on a word mode basis only.

1.3 Since the RAM uses MOS, LSI memory elements of the dynamic type to store information, a periodic refresh cycle is required to maintain the integrity of the stored information. Memory refresh is automatically accomplished by circuitry on the circuit card during usual program execution. The refresh circuitry sequences through a cycle consisting of 64 refresh operations within a period not exceeding two milliseconds.

1.4 The circuit card assemblies may be selectively located with the first address of the block on any 2K boundary. This is accomplished by setting the four address switches, A through D, contained in a switch pack on the card to the corresponding combination indicated in Figure 1.

1.5 The 4K card assembly is a depopulated version of the 8K assembly. The operational difference is determined by a strap inserted at the time of manufacture.

2. Supporting Information

2.1 Schematic Diagram 4464SD.

SECTION II - CIRCUIT DESCRIPTION

1. General

1.1 This circuit card requires the following power supply voltages:

+5 $\pm 10\%$
+5V $\pm 10\%$ Standby
+12V $\pm 10\%$ Standby
-12V $\pm 10\%$ Standby

A zener diode regulator circuit is used to derive -5V for use by the Memory Array.

1.2 The following convention is used in the circuit description to give a unique designation to each circuit in an integrated circuit package.

MLB8-4 = ML - Refers to Micro-Logic
 B8 - Refers to the package located at board location B8
 -4 - Refers to the circuit package pin number

1.3 The terms "high" and "low" are used in this description to indicate logic voltage levels; "high" represents any voltage between 2.4V and 5.5V, and "low" represents any voltage between 0.0V and 0.4V.

1.4 Signal leads are labeled with a title description of its function. A signal superscribed with a bar indicates that the signal is in the low state when the state described by the signal is present; otherwise it is in the high state.

2. General Description

2.1 The data is presented to the card via the bidirectional Telebus signals with data/address routing determined by the C0, C1, C2 bus control signals and synchronized by the MEM CLK, I/O CLK, and BUS ENABLE CLK. The decoded bus control signals produce the following functions on the memory assembly: read word, write word or byte, load address register, increment address register, and memory refresh. See Figure 2. Memory refresh may also be accomplished if the standby voltages are provided and the I/O clock is operational. Under this condition the Telebus Initialize signal is asserted to force the memory into a continuous refresh mode.

2.2 An important part of this card's operation is its ability to be selectively located at any 2K boundary. This ability to decode its own unique address is provided by a 1K word (256 x 4) ROM identified as the Card Select ROM. The four low order address signals to the Card Select ROM are presented directly from the high order bits of the address register. The four high order address signals to the Card Select ROM are determined by the proper coding of four switches on the card. The proper coding is defined on the label applied to the card.

2.3 Provision has been made to ensure accurate data retention within memory when an optional Standby-Power (+5V, +12V, -12V) source is furnished. These voltages enable the operation of the memory array and refresh circuits in the event there is a power failure if the set is equipped with a means of supplying the standby power.

3. Detailed Description

3.1 Addressing Operation

3.1.1 The address used during a read or write memory cycle is presented to the bidirectional transceivers MLC6, MLC10, MLC15, MLC20, on pins 4, 1, 12 and 15 from the Telebus. The 16 address signals are inverted by the transceivers and presented to the Address Register packages, MLC7, MLC11, MLC16 and MLC19. A load address command, LA, obtained by decoding C0, C1, C2 in package MLC3 and MLC4, moves the address to the Address Register packages. The Address Register output immediately switches state to coincide with the address input at the beginning of the load address command.

3.1.2 The memory packages require twelve address bits to access any single location in the 4096 bits of memory. These address bits are divided into two groups of six bits each which form the row and column address for the 64 x 64 memory chip matrix. The first six bits presented to the memory are row addresses while the six following address bits are column addresses.

3.1.3 The six low order address bits A1 through A6 emerging from the address register are routed to multiplexers MLC9, MLC12 and MLC17 to form the row address for the memory chip. The multiplexer input designations are 1A and 1B. Similarly, the six higher order addresses A7 through A12 are routed to the multiplexers to form the column address for the memory chip. These multiplexer input designations are 2A and 2B. The other two inputs to the multiplexers provide the memory refresh address. Six row address bits are necessary to accomplish refresh. These multiplexer input designations are 3A, 3B, 4A and 4B.

3.1.4 When Refresh Counter Enable is low, the refresh address input is applied to the multiplexer outputs. When Refresh Counter Enable is high, the Row Address and Column Address is applied to the output under command of the Mux Control signal.

3.2 Read Operation (Data to Bus from Memory)

3.2.1 A memory read cycle is performed when the decoded bus control signals command one of the three types of read operation, namely Load Address and Read (LAR), Read and Increment (RI), or Read (R). A number of conditions must be satisfied before the memory packages yield data from an addressed location. First, a row address clock and a column address clock is provided to each memory pack since the memory is dynamic.

3.2.1 (Continued)

Secondly, the memory chips must be supplied with a Chip Select signal in order to provide output data. The Chip Select signal is provided by the Card Select ROM which determines when the data being addressed resides within its own address range as indicated by the setting of the card select switches. The ROM also determines which of the two 4K memory banks will be enabled on the 8K assembly. Strap ST1 is not present in the 4K assembly and the ROM therefore only acts to control 4K of memory. Thirdly, data is read from memory only when the Read/Write Low Byte and Read/Write High Byte signals are in the read sense or high.

3.2.2 A memory cycle begins when the Row Address Strobe, RAS, switches to the low state at MLA4-3. During the initial portion of this strobe, the row addresses are read into memory. Next, the Column Address Strobe, CAS, switches to the low state at MLB1-9. During the initial portion of the strobe, the column addresses are read into memory. Approximately 200 NS later data is available and latched at the memory chip data output pin. The latched data flows to the telebus transceivers MLC6, MLC10, MLC15, and MLC20 on pins 5, 2, 11 and 14 for presentation to the bus, during the transceiver output enable time.

3.2.3 Information to the bus is regulated by a low signal on Enable A, pin 9, of transceiver packs MLC6, MLC10, MLC15 and MLC20. The transceiver output is controlled such that the data addressed during one cycle is supplied on the bus during the entire Bus Enable clock time of the following cycle. The Read F/F, MLB2-8, and the Xcvr Control F/F, MLB2-5 control the transceivers to meet the above requirement with adequate leading and lagging margins.

3.3 Write Operation (Data from Bus to Memory)

3.3.1 A memory write cycle is performed when the decoded bus signals command one of two types of write operations, namely Write Word and Increment (WWI), or Write Byte and Increment (WBI). Two of the conditions necessary for writing are the same as those needed for a read operation; those being the presence of the memory clocks and chip select signals. The third condition necessary for writing is the presence of the write signal. This signal is divided into two parts, the Read/Write Lower Byte Signal and the Read/Write High Byte Signal. When writing full words into memory, the Read/Write Low Byte and Read/Write High Byte signals are both in the write state or low. When writing in either the low or the high byte of memory, only the corresponding Read/Write signal is low.

3.3.2 The least significant address bit A0 determines whether the low or high byte should be written. A low A0 condition on the Telebus generates a Read/Write High Byte signal while a high A0 condition on the bus generates a Read/Write Low Byte signal.

3.3.3 Information to be stored in memory is presented from the Telebus to the transceivers MLC6, MLC10, MLC15, and MLC20, on pins 4, 1, 12 and 15. The output from the transceivers appears on pins 6, 3, 10 and 13, in inverted form for routing to the Data Input Latches, MLC8, MLC14, and MLB22. The information is latched with the Data Latch Clock from MLC1-8. The output from the Data Latches becomes the data input for the memory packages, MLA6 through MLA21 and MLB6 through MLB21 on pin 2.

3.3.4 The write command, either WWI or WBI, is decoded by MLC3 after receipt of the control signals through Bus Receiver MLC2. The write command is clocked into latch MLB22-12, enabling gates MLB4-3 and MLB4-6. The received CO control signal determines whether a write word or write byte operation is executed. Control CO is latched in MLB22-15 and enables gate MLB4-11 and MLB4-8 if a write byte operation is performed; similarly the gates remain disabled for a write word operation. The A0 level is likewise latched in Address Register MLC19 and used to control the write byte operation. The latched A0 directly controls an input to gate MLB4-11 and also controls an input to gate MLB4-8 after an inversion by MLC5-8. The output from MLB4-11 or MLB4-8 determines which byte will be written.

3.4 Increment Operations

3.4.1 One read function and both write functions (RI, WWI or WBI) result in the advancement of the address register to the next word location at the end of the specified read or write operation. This provision is incorporated to rapidly cycle through read/write type memory. The address counter MLC7 is advanced through the Register Increment Clock in the presence of an active Address Register Enable signal.

3.4.2 The increment associated commands are decoded through MLC3 and gate MLC4-11. The output from MLC4-11 presets the Register Enable F/F, MLB3-6, which in turn enables the low order 4 bit counter MLC7. The free running Register Increment Clock entering MLC7 advances the counter on its low to high transition during the Address Register Enable state.

3.5 Refresh

3.5.1 Since the memory chips used on this circuit card assembly are dynamic in nature, they must be refreshed. Reading information at an addressed location is non-destructive and refreshes one row of memory. Total refresh is accomplished by performing one internal read cycle on each of the 64 low order addresses every two milliseconds. The memory is refreshed whether Chip Select, pin 5, is high or low. A dedicated refresh cycle is initiated whenever there is a NOP on the Telebus. A NOP is decoded by package MLC3, producing a low output on pin 13. This signal presets the Refresh F/F, MLB3-9, to a high state.

3.5.2 A high output from the Refresh F/F decontrols the Card Select ROM, MLA3 on pins 13 and 14, forcing MLA3-11 and MLA3-10 high to disable the Chip Select signal to pin 13 of the RAM packs. Multiplexers MLC9, MLC12, and MLC17 which control the RAM address is switched to yield the refresh counter address to the RAM packages. The Refresh F/F output, when inverted by MLC1-6, provides an enable signal to the Refresh Counters, MLC13 and MLC18, which allows the counters to advance to the next address location at the end of the refresh cycle through the action of the Register Increment clock. The refresh counters are thus positioned to the next refresh address when the current refresh cycle is completed.

3.6 Standby Power

3.6.1 Provisions have been made on the assembly to power the memory packs and some peripheral logic from a secondary power source, collectively known as the Standby Voltages, in the event that this function is provided within the controller. Maintenance of the +5V Standby, +12V Standby, and -12V Standby voltages in the event of a main power failure would insure accurate data retention in the memory array.

3.6.2 Two other provisions are necessary to maintain memory. The Telebus I/O clock must continue to operate at the normal rate or at a rate which will assure 64 complete cycles within 2 milliseconds. Additionally the Initialize Bus control must be placed into initialized state or in an off state. The Initialize signal is detected by a discrete amplifier which controls the clocked input of the Refresh F/F MLB3. When Initialize is asserted, the flip-flop is forced into a continuous refresh mode, thereby maintaining memory data as described in the Refresh section.

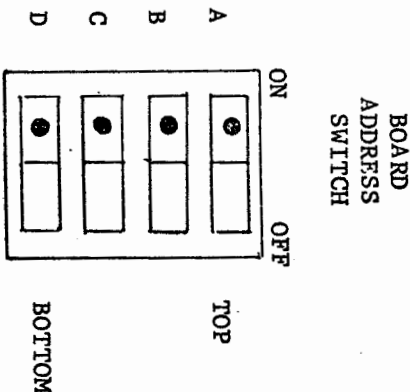
MEMORY CARD ADDRESSING

ADDRESS LABEL

MEM START ADDRESS	DEC	OCTAL	BOTTOM	TOP
0K	00K	0	0	0
2	10	0	0	1
4	20	0	0	0
6	30	0	0	1
8	40	0	1	0
10	50	0	1	0
12	60	0	1	1
14	70	0	1	1
16	100	1	0	0
18	110	1	0	1
20	120	1	0	0
22	130	1	0	1
24	140	1	1	0
26	150	1	1	0
28	160	1	1	1
30	170	1	1	1

0 = DOWN OR "ON"
1 = UP OR "OFF"

FIGURE 1



MEMORY CONTROLS AND FUNCTIONS

DECODER INPUT CONTROLS			DECODED FUNCTION	READ/WRITE MEMORY OPERATION
C2	C1	C0		
0	0	0	NOP	REFRESH RAM, THEN INCREMENT REFRESH COUNTER.
0	0	1	RDV	-----
0	1	0	LAR	LOAD ADDRESS REGISTER, READ THE DATA, OUTPUT DATA DURING NEXT CYCLE.
0	1	1	LA	LOAD ADDRESS REGISTER.
1	0	0	WWI	WRITE WORD CONTAINED IN DATA INPUT LATCH AT ADDRESSED LOCATION, THEN INCREMENT ADDRESS.
1	0	1	WBI	WRITE BYTE CONTAINED IN DATA INPUT LATCH AT ADDRESSED LOCATION, THEN INCREMENT ADDRESS.
1	1	0	RI	READ DATA AT ADDRESSED LOCATION, INCREMENT ADDRESS, OUTPUT DATA DURING NEXT CYCLE.
1	1	1	R	READ DATA AT ADDRESSED LOCATION AND OUTPUT DURING NEXT CYCLE.

FIGURE 2

4500CD

Sheet 1

Teletype Corporation Circuit Description

4500CD
Issue 1
Sheet 2

CIRCUIT DESCRIPTION FOR THE
410500 SERIES ERASABLE PROGRAMMABLE
READ ONLY MEMORY CIRCUIT CARDS

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SECTION II - CIRCUIT DESCRIPTION

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1. General
2. General Description
3. Detailed Description

4
4
5.[illegible]

SECTION I - USER INFORMATION

1.0 GENERAL

1.1 The 410506 through 410540 series Erasable Programmable ROM (EPROM) Circuit Cards function as read only memory in the 40C400 Controller. These cards come in a variety of memory configurations dependent upon application and program need. The maximum card capability is 10K (10240) words of 16 bits. Application which requires less than the full 10K capability may build memory in 1K or 2K word increments. It must be noted, however, that the circuit card addressing operates over full 2K word blocks rather than 1K word blocks so that a card would respond to addresses in the full 2K block even through 1K words of program resided in a block.

1.2 Two basic card assemblies are used to construct the above series. The 410504 Circuit Card Assembly is a basic assembly which contains no memory. Memory packs are added to sockets to fit the application. The 410504 Assembly contains Telebus pull-up resistors which are required to generate the bus "high" state. The companion 410505 Circuit Card Assembly is identical to the 410504 Assembly with the exception that no bus pull-up resistors are provided. Each 40C400 must have only one circuit card with bus pull-up resistors. When memory requirements exceed one circuit card, additional memory is constructed on cards without pull-up resistors.

1.3 The 410504 Card should also contain 2K words of EPROM starting at octal address 170000 which is dedicated for system use. Therefore the maximum user application area on the 410504 base card is 8K words of memory.

1.4 Applications with 8K or less of user memory will select the 410504 to construct either 0K, 2K, 4K, 6K or 10K of application program. The remaining 2K on the card should be dedicated to system operation. Where the memory need exceeds 8K of program, the 10K 410505 base card is selected to construct the application with the remaining program need constructed from the 410504 Card above. In this manner two EPROM cards allow up to 18K of application memory.

1.5 The card address select switch allows the application program to be located on any 2K boundary in the 32K word memory map. The four miniature toggle switches within the switch assembly determine 1 of 16 2K starting address boundaries. The addressing range to which the card responds is determined by a 256 x 4 ROM pack in the control logic of the circuit card. Figure 2 lists the appropriate part number for an addressing range of 2K, 4K, 6K, 8K or 10K of user application program. The system area memory slot is also decoded by this part at octal address 170000. Once the program length is determined, consult the table on figure 2 for the appropriate part number.

2. SUPPORTING INFORMATION

2.1 Schematic Diagram 4500SD.

SECTION II - CIRCUIT DESCRIPTION

1. GENERAL

1.1 This circuit card requires the following power supply voltages:

+5V $\pm$ 10%
+5V $\pm$ 10% Standby
+12V $\pm$ 10%
-12V $\pm$ 10%

1.2 The following convention is used in the circuit description to give a unique designation to each circuit in an integrated circuit package.

MLA1-3

ML - Denotes micrologic
A1 - Refers to the IC package located at
board location A1
-3 - Refers to the pin number of the
IC circuit

One entire IC gate may also be referred to by its position on the board and its output pin such as MLC5-6.

1.3 The terms "high" and "low" are used in this description to indicate logic voltage levels. High represents any voltage level between 2.4V and 5.5V, and low represents any voltage between 0.0V and 0.4V.

1.4 Signal leads are labeled with a title descriptive of its function. A signal superscribed with a bar indicates that the signal is in the low state when the state described by the signal is present; otherwise it is in the high state.

2. GENERAL DESCRIPTION

2.1 The Telebus signals which are required and to which this circuit card assembly responds are the following:

<u>FUNCTION</u>	<u>SYMBOL</u>
16 Data/Address Bidirectional Signals	D/A
3 Control Signals	C0, C1, C2
2 Clocks:	
Bus Enable Clock	Bus En Clk
Memory Clock	Mem Clk

2.1 (Continued)

The system card contains bus pull up resistors on all of the above leads. Additionally this card assembly provides bus pull up resistors on the following Telebus leads:

- A. Interrupt (Intr)
- B. Device B Enable
- C. Device A Enable
- D. Initialize
- E. Trap
- F. I/O CLK

2.2 A typical operational cycle proceeds in the following manner. The binary information residing on the bus Data/Address leads is received by the bus transceivers which in turn output the information as an address to the address latch. The low order address leads A1 through A10 directly address the EPROM IC packs. A0 is not used as an address since its function is to determine the byte address, whereas full words are addressed in ROM. Address levels A11 and the outputs from the card select ROM are used to generate a one of ten column selects for the EPROM array in conjunction with addresses A12 through A15 which determine whether a particular memory board has been selected. Output data from the EPROM is clocked into the output latches and then to the input of the bus transceivers for presentation on the bus during the next cycle.

2.3 The address latch loads the address from the bus whenever a Load Address (LA) or Load Address and Read (LAR) control signal is decoded. Data obtained from the EPROM after the access time has elapsed is clocked into the output latches and presented to the bus on the Load Address and Read command only. This data exists on the bus during the bus enable portion of the cycle following the Load Address and Read command along with margin on either side of the bus enable window.

3. DETAILED DESCRIPTION

3.1 Typical Read Cycle

3.1.1 The 16 Data/Address signals on the Telebus are received by the bi-directional, data inverting transceiver packages MLC3, MLC4, MLC5 and MLC6 on input/output pins 4, 1, 12 and 15. The transceivers output the information as an address on pins 6, 3, 10 and 13 respectively, in inverted form.

3.1.2 The low order address signals $\overline{A1}$ through $\overline{A11}$ from the transceivers are presented to the Address Latches, packages MLB4 and MLB5, on pins 3, 4, 6, 11, 13 and 14. The high order address signals A12 through A15 are presented to package MLA2, pins 4, 6, 11 and 13. The address is clocked into the Address Latches on pin 9 with a low to high transition of the Load Address or Load Address and Read command signal. These two commands are decoded by MLC1 under control of the Bus Enable Clock signal on MLC1-2. The control signals C0, C1 and C2 are routed to MLC1 through bus receiver MLC2.

3.1.3 The low order latched addresses A1 through A10 originating from packages MLB4 and MLB5 on pins 2, 5, 7, 10, 12 and 15, are presented directly to the EPROMs as an address for 1024 bits. The high order latched addresses A11 through A15 are handled in the following manner. The four highest order address signals A12, A13, A14 and A15, in combination with the user prescribe setting of the card select switch, determines the output from the Card Select ROM, MLA3-9. A low output from the Card Select ROM indicates that the card assembly has been selected and will output data if a LAR command has been decoded. Outputs MLA3-12, 11 and 10 from the Card Select ROM are used as inputs to the column decoder MLA4. Address A11 acts as the low order input to the column decoder.

3.1.4 The column decoder MLA4 selects the pair of EPROMs from which the data word is read. These decoder outputs drive the Chip Select leads of the EPROM. When selected, the EPROM in the upper row provides the low order data byte while the EPROM in the lower row provides the high order data byte.

3.1.5 The Card Select ROM MLA3 determines the address range to which each card responds. A unique EPROM card assembly may be constructed for the system card only or the 2K, 4K, 6K and 8K User/System, or the 10K User card. Figure 2 describes the card layout along with the appropriate MLA3 ROM part number needed for the memory variations. MLA3-9 inverted by MLB2-3 controls the operation of the Read F/F MLB1-9. A low output on MLA3-9 allows the Read F/F to function during the LAR command from decoder MLC1-11. The MLB1-9 output controls the Xcvr Output F/F MLB1-5, which in turn regulates the output interval for transceiver packages MLC3, MLC4, MLC5 and MLC6.

MEMORY CARD ADDRESSING

MEM START ADDRESS DEC	OCTAL	BOTTOM	TOP
0K	00K	0	0
2	10	0	0
4	20	0	0
6	30	0	0
8	40	0	0
10	50	0	0
12	60	0	0
14	70	0	0
16	100	1	0
18	110	1	0
20	120	1	0
22	130	1	0
24	140	1	0
26	150	1	0
28	160	1	0
30	170	1	0

0 = DOWN OR "ON"
1 = UP OR "OFF"

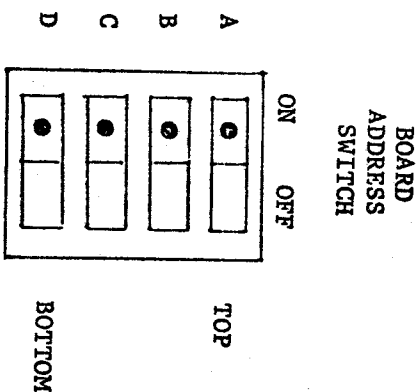
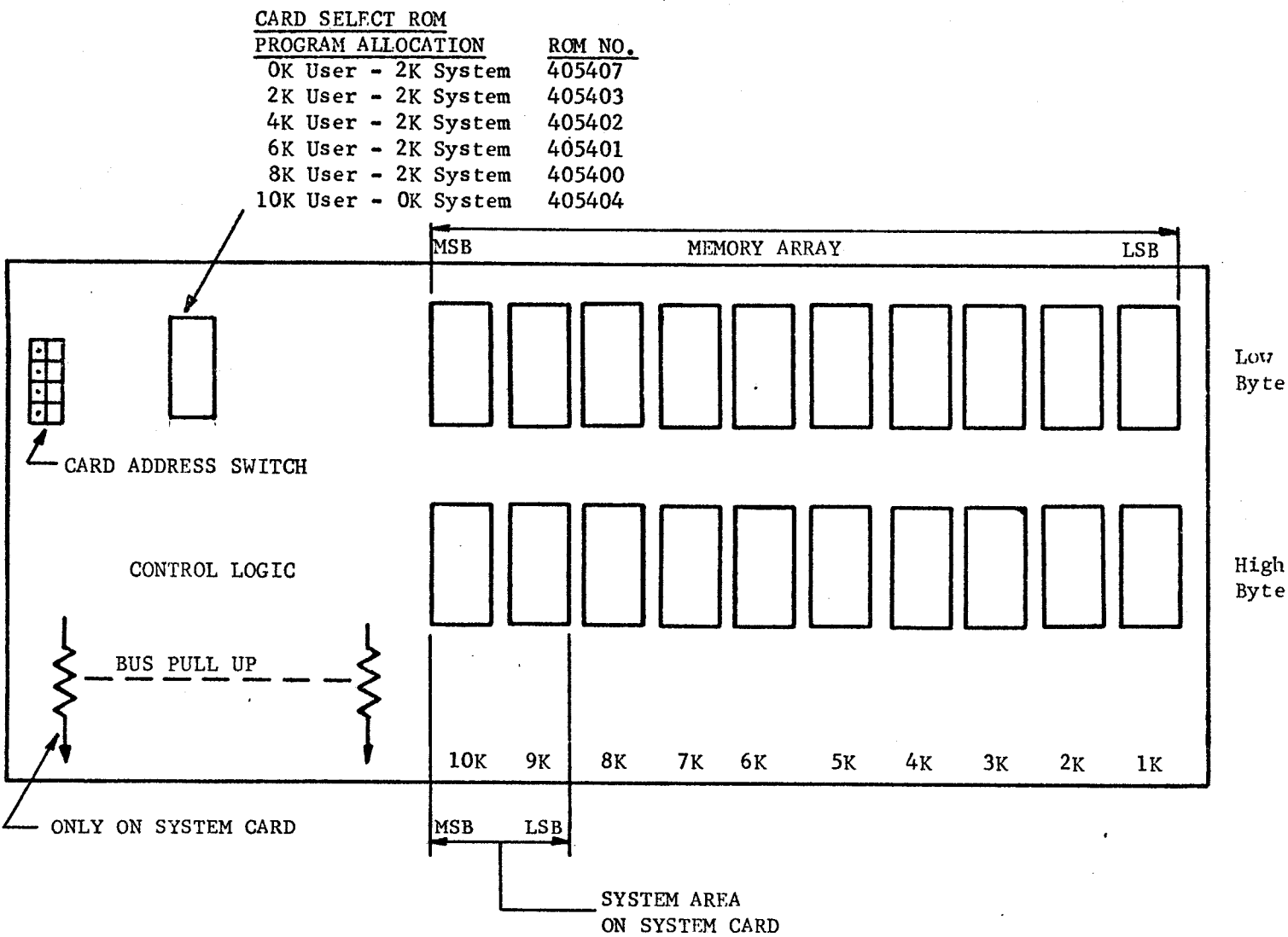
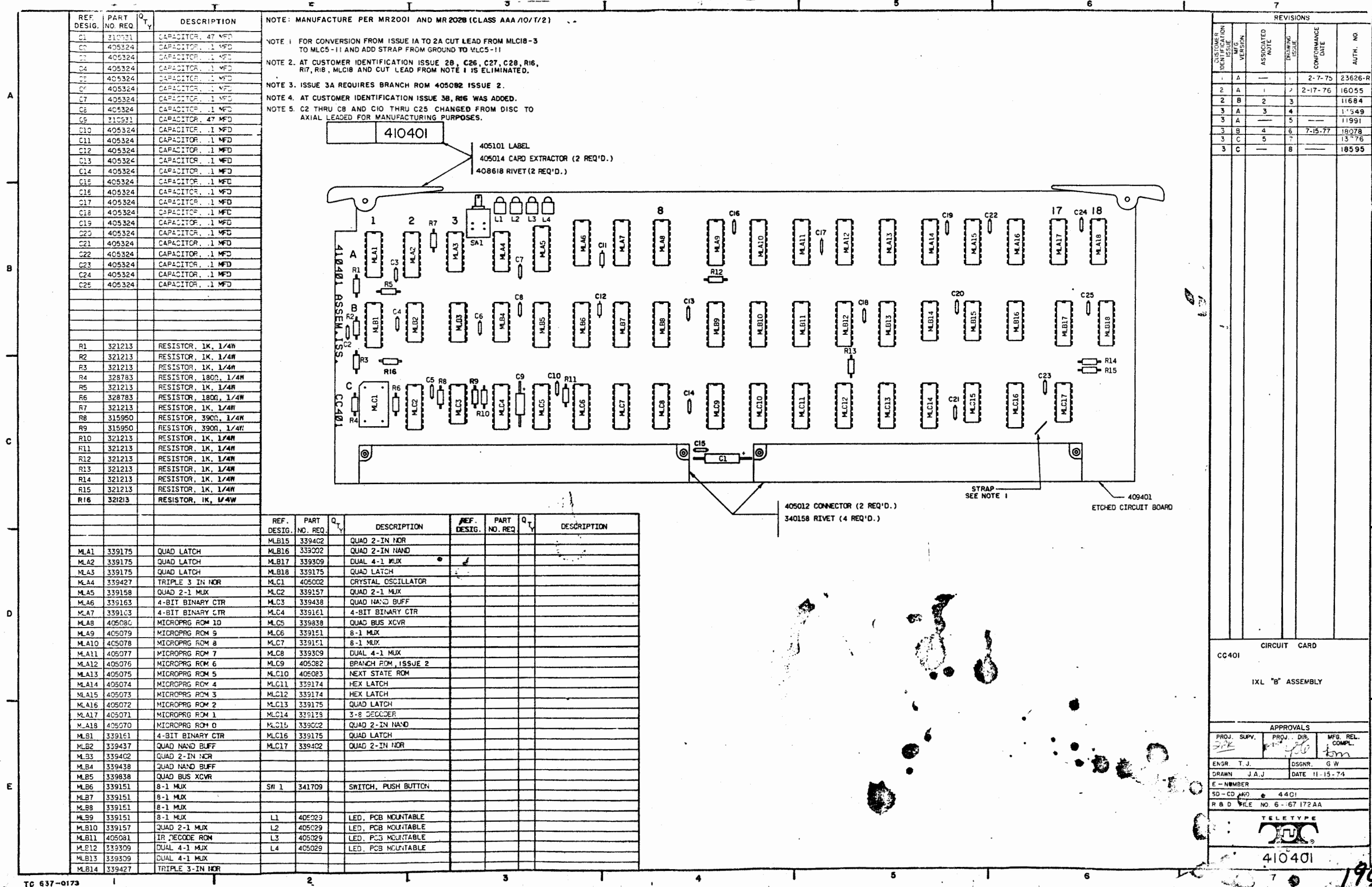


FIGURE 1



MEMORY CIRCUIT CARD

FIGURE 2



NOTE: MANUFACTURE PER MR2001 AND MR2028 (CLASS AAA /10/T/2)

NOTE 1. FOR CONVERSION FROM ISSUE 1A TO 2A CUT LEAD FROM MLC18-3 TO MLC5-11 AND ADD STRAP FROM GROUND TO MLC5-11

NOTE 2. AT CUSTOMER IDENTIFICATION ISSUE 28, C26, C27, C28, R16, R17, R18, MLC18 AND CUT LEAD FROM NOTE 1 IS ELIMINATED.

NOTE 3. ISSUE 3A REQUIRES BRANCH ROM 405082 ISSUE 2.

NOTE 4. AT CUSTOMER IDENTIFICATION ISSUE 38, R16 WAS ADDED.

NOTE 5. C2 THRU C8 AND C10 THRU C25 CHANGED FROM DISC TO AXIAL LEADED FOR MANUFACTURING PURPOSES.

REVISIONS					
CUSTOMER IDENTIFICATION	ISSUE	DATE	ASSOCIATED NOTE	CONFORMANCE DATE	AUTH. NO.
1	A	2-7-75			23626-R
2	A	2-17-76			16055
2	B				11684
3	A				11549
3	A				11991
3	B				18078
3	C				13776
3	C				18595

REF. DESIG.	PART NO. REQ.	QTY	DESCRIPTION
C1	310931		CAPACITOR, .47 MFD
C2	405324		CAPACITOR, .1 MFD
C3	405324		CAPACITOR, .1 MFD
C4	405324		CAPACITOR, .1 MFD
C5	405324		CAPACITOR, .1 MFD
C6	405324		CAPACITOR, .1 MFD
C7	405324		CAPACITOR, .1 MFD
C8	405324		CAPACITOR, .1 MFD
C9	310931		CAPACITOR, .47 MFD
C10	405324		CAPACITOR, .1 MFD
C11	405324		CAPACITOR, .1 MFD
C12	405324		CAPACITOR, .1 MFD
C13	405324		CAPACITOR, .1 MFD
C14	405324		CAPACITOR, .1 MFD
C15	405324		CAPACITOR, .1 MFD
C16	405324		CAPACITOR, .1 MFD
C17	405324		CAPACITOR, .1 MFD
C18	405324		CAPACITOR, .1 MFD
C19	405324		CAPACITOR, .1 MFD
C20	405324		CAPACITOR, .1 MFD
C21	405324		CAPACITOR, .1 MFD
C22	405324		CAPACITOR, .1 MFD
C23	405324		CAPACITOR, .1 MFD
C24	405324		CAPACITOR, .1 MFD
C25	405324		CAPACITOR, .1 MFD
R1	321213		RESISTOR, 1K, 1/4W
R2	321213		RESISTOR, 1K, 1/4W
R3	321213		RESISTOR, 1K, 1/4W
R4	328783		RESISTOR, 180Ω, 1/4W
R5	321213		RESISTOR, 1K, 1/4W
R6	328783		RESISTOR, 180Ω, 1/4W
R7	321213		RESISTOR, 1K, 1/4W
R8	315950		RESISTOR, 390Ω, 1/4W
R9	315950		RESISTOR, 390Ω, 1/4W
R10	321213		RESISTOR, 1K, 1/4W
R11	321213		RESISTOR, 1K, 1/4W
R12	321213		RESISTOR, 1K, 1/4W
R13	321213		RESISTOR, 1K, 1/4W
R14	321213		RESISTOR, 1K, 1/4W
R15	321213		RESISTOR, 1K, 1/4W
R16	321213		RESISTOR, 1K, 1/4W

REF. DESIG.	PART NO. REQ.	QTY	DESCRIPTION	REF. DESIG.	PART NO. REQ.	QTY	DESCRIPTION
MLA1	339175		QUAD LATCH	MLB15	339402		QUAD 2-IN NOR
MLA2	339175		QUAD LATCH	MLB16	339002		QUAD 2-IN NAND
MLA3	339175		QUAD LATCH	MLB17	339309		DUAL 4-1 MUX
MLA4	339427		TRIPLE 3 IN NOR	MLB18	339175		QUAD LATCH
MLA5	339158		QUAD 2-1 MUX	MLC1	405002		CRYSTAL OSCILLATOR
MLA6	339163		4-BIT BINARY CTR	MLC2	339157		QUAD 2-1 MUX
MLA7	339163		4-BIT BINARY CTR	MLC3	339438		QUAD NAND BUFF
MLA8	405086		MICROPRG ROM 10	MLC4	339161		4-BIT BINARY CTR
MLA9	405079		MICROPRG ROM 9	MLC5	339838		QUAD BUS XCVR
MLA10	405078		MICROPRG ROM 8	MLC6	339151		8-1 MUX
MLA11	405077		MICROPRG ROM 7	MLC7	339151		8-1 MUX
MLA12	405076		MICROPRG ROM 6	MLC8	339309		DUAL 4-1 MUX
MLA13	405075		MICROPRG ROM 5	MLC9	405082		BRANCH ROM, ISSUE 2
MLA14	405074		MICROPRG ROM 4	MLC10	405083		NEXT STATE ROM
MLA15	405073		MICROPRG ROM 3	MLC11	339174		HEX LATCH
MLA16	405072		MICROPRG ROM 2	MLC12	339174		HEX LATCH
MLA17	405071		MICROPRG ROM 1	MLC13	339175		QUAD LATCH
MLA18	405070		MICROPRG ROM 0	MLC14	339178		3-8 DECODER
MLB1	339161		4-BIT BINARY CTR	MLC15	339002		QUAD 2-IN NAND
MLB2	339437		QUAD NAND BUFF	MLC16	339175		QUAD LATCH
MLB3	339402		QUAD 2-IN NOR	MLC17	339402		QUAD 2-IN NOR
MLB4	339438		QUAD NAND BUFF				
MLB5	339838		QUAD BUS XCVR				
MLB6	339151		8-1 MUX	SW 1	341709		SWITCH, PUSH BUTTON
MLB7	339151		8-1 MUX				
MLB8	339151		8-1 MUX				
MLB9	339151		8-1 MUX	L1	405029		LED, PCB MOUNTABLE
MLB10	339157		QUAD 2-1 MUX	L2	405029		LED, PCB MOUNTABLE
MLB11	405081		IR DECODE ROM	L3	405029		LED, PCB MOUNTABLE
MLB12	339309		DUAL 4-1 MUX	L4	405029		LED, PCB MOUNTABLE
MLB13	339309		DUAL 4-1 MUX				
MLB14	339427		TRIPLE 3-IN NOR				

CIRCUIT CARD

CC401

IXL "B" ASSEMBLY

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.
ENGR. T.J.	DSGMR. G.W.	
DRAWN J.A.J.	DATE 11-15-74	
E-NUMBER		
SD - CD AND	4401	
R & D FILE NO.	6-67 172AA	

TELETYPE

410401

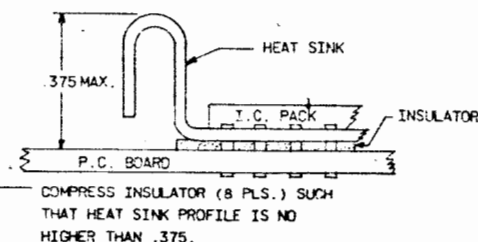
410 406

405014 EXTRACTOR (2 PLS.)
408618 RIVET (2 PLS.)

NOTE: 2. ON CUSTOMER I.D. ISSUE 68, THE VALUE OF R1-R8 AND R96 IS 12K.

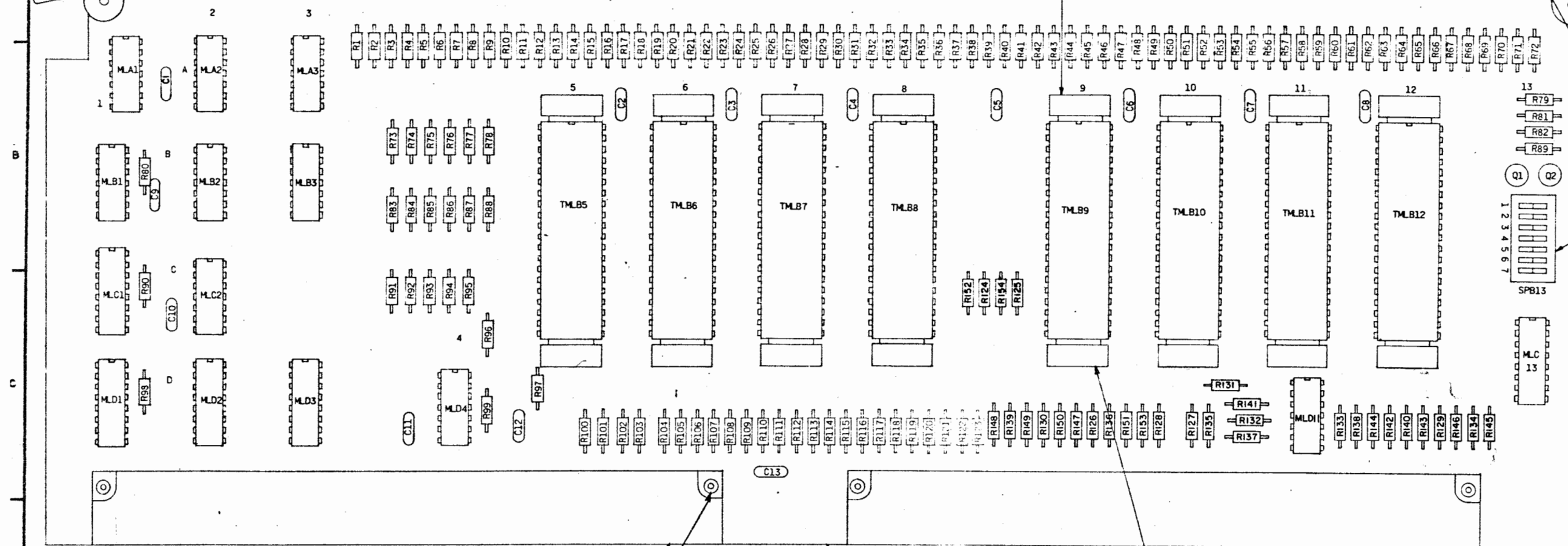
NOTE: 3 ON CUSTOMER I. D. ISSUE 6C, THE VALUE OF RI-R8 AND R96 IS 10K.

NOTE: 4 196113 ROLL PIN CHANGED TO 408618 RIVET.



ORIENT SWITCH PACK
WITH SWITCH 1 TO TOP
OF BOARD AS SHOWN.

REVISIONS						
CONTRACTOR'S IDENTIFICATION NUMBER	ISSUE M/G VERSION	ASSOCIATED NOTE	DRAWING ISSUE	CONFORMANCE (DATE)	AUTH. NO.	
6	B	1	7	12-8-75	14776	
6	C	2	8	3-1-76	14992	
6	D	3	9	3-15-76	11671	
6	D	4	10	—	11991	
6	D	—	11	7-7-77	13555	
6	D	—	12	—	18595	



405012 CONNECTOR, 71 PIN (2 PLS.)
340158 RIVET (4 PLS.) -----

- 409406 BOARD, ETCHED CIRCUIT

403446 HEAT SINK W/INSULATOR (8 PLS.)

REF. DESIG.	PART NO. REQ.	QTY.	DESCRIPTION	REF. DESIG.	PART NO. REQ.	QTY.	DESCRIPTION	REF. DESIG.	PART NO. REQ.	QTY.	DESCRIPTION	REF. DESIG.	PART NO. REQ.	QTY.	DESCRIPTION	REF. DESIG.	PART NO. REQ.	QTY.	DESCRIPTION
MLA1	339416	1	HEX. DRIVER	C1-C13	319999	13	CAPACITOR, .01 uf	R99			SAME AS R73	R129	328737	4	RESISTOR, 120K				
MLA2	326858	2	QUAD BUFFER					P100				R130			SAME AS R9				
MLA3			SAME AS MLA2					P102	323148	15	RESISTOR, 18K	P130	315985	4	RESISTOR, 5.1K				
MLB1	339002	2	QUAD GATE	SPB13	341807	1	SWITCH, 7 POS.	P103	320226	8	RESISTOR, 3.9K	R133			SAME AS P102				
MLB2	339417	3	HEX DRIVER					P104	318803	4	RESISTOR, 2.4K	R134			SAME AS R129				
MLB3			SAME AS MLB2					P105			SAME AS R103	R135							
TMLB5	344981	4	ASSEMBLY, IC	Q1	323934	1	TRANSISTOR, 2N3555	P106				R136			SAME AS R9				
TMLB6			SAME AS TMLB5	Q2	324144	1	TRANSISTOR, 2N4121	P108			SAME AS R100	R138			SAME AS R129				
TMLB7			SAME AS TMLB5					P109			SAME AS P103	R139			SAME AS R9				
TMLB8			SAME AS TMLB5					P110			SAME AS P104	P140			SAME AS R102				
TMLB9	344979	4	ASSEMBLY, IC	R1-R8	300092	9	RESISTOR, 6.8K	P111			SAME AS R103	P141			SAME AS R132				
TMLB10			SAME AS TMLB9	R9-R72	315956	81	RESISTOR, 2.7K	P112				P142			SAME AS R129				
TMLB11			SAME AS TMLB9	R73-R78	321213	19	RESISTOR, 1K	P114			SAME AS R100	P143							
TMLB12			SAME AS TMLB9	R79	319801	1	RESISTOR, 47K	R115			SAME AS R103	R146	315955	4	RESISTOR, 2.2K				
MLC1	339161	1	4 BIT COUNTER	R80			SAME AS R73	P116			SAME AS P104	P147							
MLC2			SAME AS MLC2	R81	215972	2	RESISTOR, 22K	P117			SAME AS R103	P154			SAME AS R9				
MLC13	404161	1	CMOS 4 BIT COUNTER	R82	320275	1	RESISTOR, 10K	R118				R137			SAME AS R132				
MLC1	339837	3	HEX RECEIVER	R83-R88			SAME AS R73	R120			SAME AS P100	R131			SAME AS R132				
MLD2			SAME AS MLC1	R89			SAME AS R81	R121			SAME AS P103								
MLD3			SAME AS MLC1	R90	315959	1	RESISTOR, 4.7K	R122			SAME AS P104								
MLD4			SAME AS MLC1	R91-R95			SAME AS R73	R123			SAME AS R103								
MLD11	404239	1	QUAD COMPARATOR	R96			SAME AS R1	R124											
				R97			SAME AS R9	R127			SAME AS R9								
				R98	328788	1	RESISTOR, 330	P128			SAME AS P102								

CIRCUIT CARD

CC 406

SSI INPUT / OUTPUT
CIRCUIT CARD ASSEMBLY

APPROVALS

PROJ. SUPV. (1)	PROJ. DIR.	MFG. REL. COMPL. AJS
--------------------	------------	----------------------------

ENGR S. J. K.	DSGMR
DRAWN T. G. P.	DATE

E - NUMBER
SD - CD NO. 4406

R & D FILE NO 1-167.172AA

TELETYPE

410406 (3 OF 3)

A

B

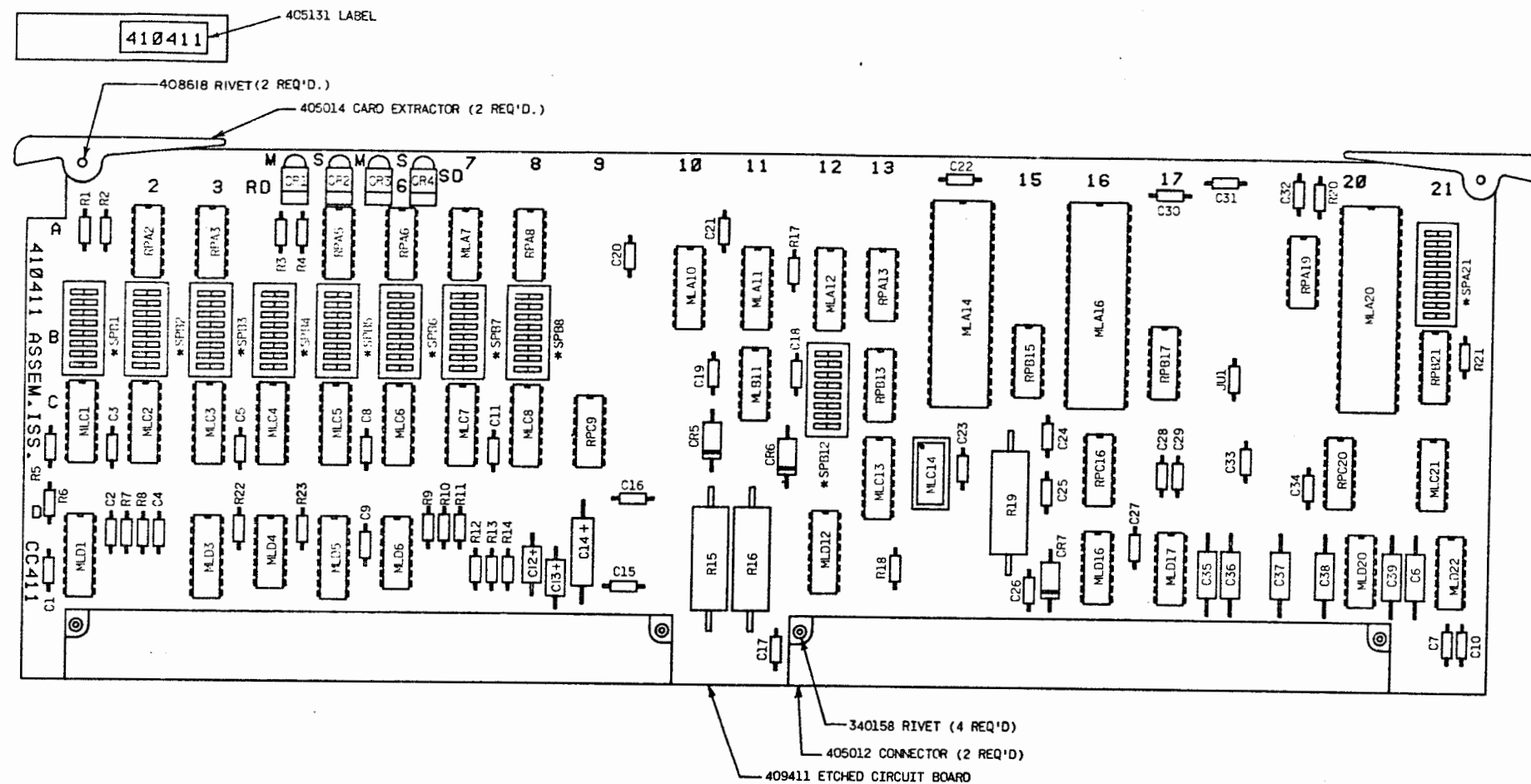
C

D

E

REF. DESIG.	PART NO. REQ.	QTY	DESCRIPTION
C1	405324		CAPACITOR, .1 uF
C2	405324		CAPACITOR, .1 uF
C3	405324		CAPACITOR, .1 uF
C4	405324		CAPACITOR, .1 uF
C5	405324		CAPACITOR, .1 uF
C6	181700		CAPACITOR, .001 uF
C7	405324		CAPACITOR, .1 uF
C8	405324		CAPACITOR, .1 uF
C9	405324		CAPACITOR, .1 uF
C10	405324		CAPACITOR, .1 uF
C11	405324		CAPACITOR, .1 uF
C12	337335		CAPACITOR, 15 uF
C13	337335		CAPACITOR, 15 uF
C14	310931		CAPACITOR, 47 uF
C15	405324		CAPACITOR, .1 uF
C16	405324		CAPACITOR, .1 uF
C17	405324		CAPACITOR, .1 uF
C18	405324		CAPACITOR, .1 uF
C19	405324		CAPACITOR, .1 uF
C20	405324		CAPACITOR, .1 uF
C21	405324		CAPACITOR, .1 uF
C22	405324		CAPACITOR, .1 uF
C23	405324		CAPACITOR, .1 uF
C24	405324		CAPACITOR, .1 uF
C25	335903		CAPACITOR, 220 pF
C26	405324		CAPACITOR, .1 uF
C27	405324		CAPACITOR, .1 uF
C28	335903		CAPACITOR, 220 pF
C29	335903		CAPACITOR, 220 pF
C30	405324		CAPACITOR, .1 uF
C31	405324		CAPACITOR, .1 uF
C32	405324		CAPACITOR, .1 uF
C33	405324		CAPACITOR, .1 uF
C34	405324		CAPACITOR, .1 uF
C35	181700		CAPACITOR, .001 uF
C36	181700		CAPACITOR, .001 uF
C37	181700		CAPACITOR, .001 uF
C38	181700		CAPACITOR, .001 uF
C39	181700		CAPACITOR, .001 uF
R1	328783		RESISTOR, 180, 1/4W
R2	328783		RESISTOR, 180, 1/4W
R3	328783		RESISTOR, 180, 1/4W
R4	328783		RESISTOR, 180, 1/4W
R5	320276		RESISTOR, 470, 1/4W
R6	320276		RESISTOR, 470, 1/4W
R7	321213		RESISTOR, 1K, 1/4W
R8	321213		RESISTOR, 1K, 1/4W
R9	320276		RESISTOR, 470, 1/4W
R10	320276		RESISTOR, 470, 1/4W
R11	320276		RESISTOR, 470, 1/4W
R12	315959		RESISTOR, 4.7K, 1/4W
R13	315959		RESISTOR, 4.7K, 1/4W
R14	315959		RESISTOR, 4.7K, 1/4W
R15	311027		RESISTOR, 60, 5W
R16	311027		RESISTOR, 60, 5W
R17	300062		RESISTOR, 6.8K, 1/4W
R18	320276		RESISTOR, 470, 1/4W
R19	311027		RESISTOR, 60, 5W
R20	320276		RESISTOR, 470, 1/4W
R21	315959		RESISTOR, 4.7K, 1/4W
R22	321213		RESISTOR, 1K, 1/4W
R23	321213		RESISTOR, 1K, 1/4W
MLA7	339404		HEX INVERTER
MLA10	339838		QUAD TRANSCEIVER
MLA11	339838		QUAD TRANSCEIVER
MLA12	339347		6 BIT COMPARATOR
MLA14	342292		PIU / SID
MLA16	342290		CIU-RECEIVER
MLA20	342291		CIU-TRANSMITTER
MLB11	339404		HEX INVERTER
MLC1	339251		8 INTO 1 MUX
MLC2	339251		8 INTO 1 MUX
MLC3	339251		8 INTO 1 MUX
MLC4	339251		8 INTO 1 MUX
MLC5	339251		8 INTO 1 MUX
MLC6	339251		8 INTO 1 MUX
MLC7	339251		8 INTO 1 MUX
MLC8	339251		8 INTO 1 MUX
MLC13	339161		4 BIT COUNTER
MLC14	405005		CRYSTAL OSCILLATOR

NOTE: MANUFACTURE PER MR2001 AND MR2028 (CLASS AAA/IO/T/2)

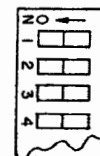


REF. DESIG.	PART NO. REQ.	QTY	DESCRIPTION
MLC21	335528		EIA LINE DRIVER
MLD1	339837		HEX RECEIVER
MLD3	339837		HEX RECEIVER
MLD4	339433		QUAD NAND BUFFER
MLD5	339138		1 OF 8 DECODER
MLD6	339002		QUAD 2 IN NAND
MLD12	339347		6 BIT COMPARATOR
MLD16	335529		EIA LINE RECEIVER
MLD17	335529		EIA LINE RECEIVER
MLD20	335529		EIA LINE RECEIVER
MLD22	335528		EIA LINE DRIVER
RPA2	341733		RESISTOR PKG., 6.8K
RPA3	341733		RESISTOR PKG., 6.8K
RPA5	341733		RESISTOR PKG., 6.8K
RPA6	341733		RESISTOR PKG., 6.8K
RPA8	341733		RESISTOR PKG., 6.8K
RPA13	341827		RESISTOR PKG., 1K
RPA19	341733		RESISTOR PKG., 6.8K
RPB13	341733		RESISTOR PKG., 6.8K
RPB15	341830		RESISTOR PKG., 4.7K
RPB17	341830		RESISTOR PKG., 4.7K
RPB21	341830		RESISTOR PKG., 4.7K
RPC9	341830		RESISTOR PKG., 4.7K
RPC16	341827		RESISTOR PKG., 1K
RPC20	341827		RESISTOR PKG., 1K

REF. DESIG.	PART NO. REQ.	QTY	DESCRIPTION
SPA21	341809		SWITCH, 9 POSITION
SPB1	341808		SWITCH, 8 POSITION
SPB2	341808		SWITCH, 8 POSITION
SPB3	341808		SWITCH, 8 POSITION
SPB4	341808		SWITCH, 8 POSITION
SPB5	341808		SWITCH, 8 POSITION
SPB6	341808		SWITCH, 8 POSITION
SPB7	341808		SWITCH, 8 POSITION
SPB8	341808		SWITCH, 8 POSITION
SPB12	341808		SWITCH, 8 POSITION
CR1	405029		LIGHT EMITTING DIODE
CR2	405029		LIGHT EMITTING DIODE
CR3	405029		LIGHT EMITTING DIODE
CR4	405029		LIGHT EMITTING DIODE
CR5	405214		ZENER DIODE, 6.2V
CR6	405214		ZENER DIODE, 6.2V
CR7	405214		ZENER DIODE, 6.2V
JU1	336470		STRAP
	340158		RIVET, TUBULAR
	405012		CONNECTOR
	409411		BOARD
	408618		RIVET
	405014		EXTRACTOR
	405131		LABEL

NOTES:

- FOR CONVERSION FROM CUSTOMER I.D. ISSUE 1A TO ISSUE 1B, BOARD ISSUE 2A WITH RE-ROUTED LANDS IS USED.
- * ORIENT SWITCH PACKS WITH SWITCH 1 TO TOP OF BOARD (IO-PLS.) AS SHOWN. ON SOME EARLY CARD ASSEMBLIES, THE ON POSITION OF THE SWITCH MAY THEN BE TO THE RIGHT INSTEAD OF THE LEFT. ALWAYS OBSERVE THE ON DIRECTION OF THE SWITCH WHEN FOLLOWING PROGRAMMING INSTRUCTIONS.



SIMILAR TO:

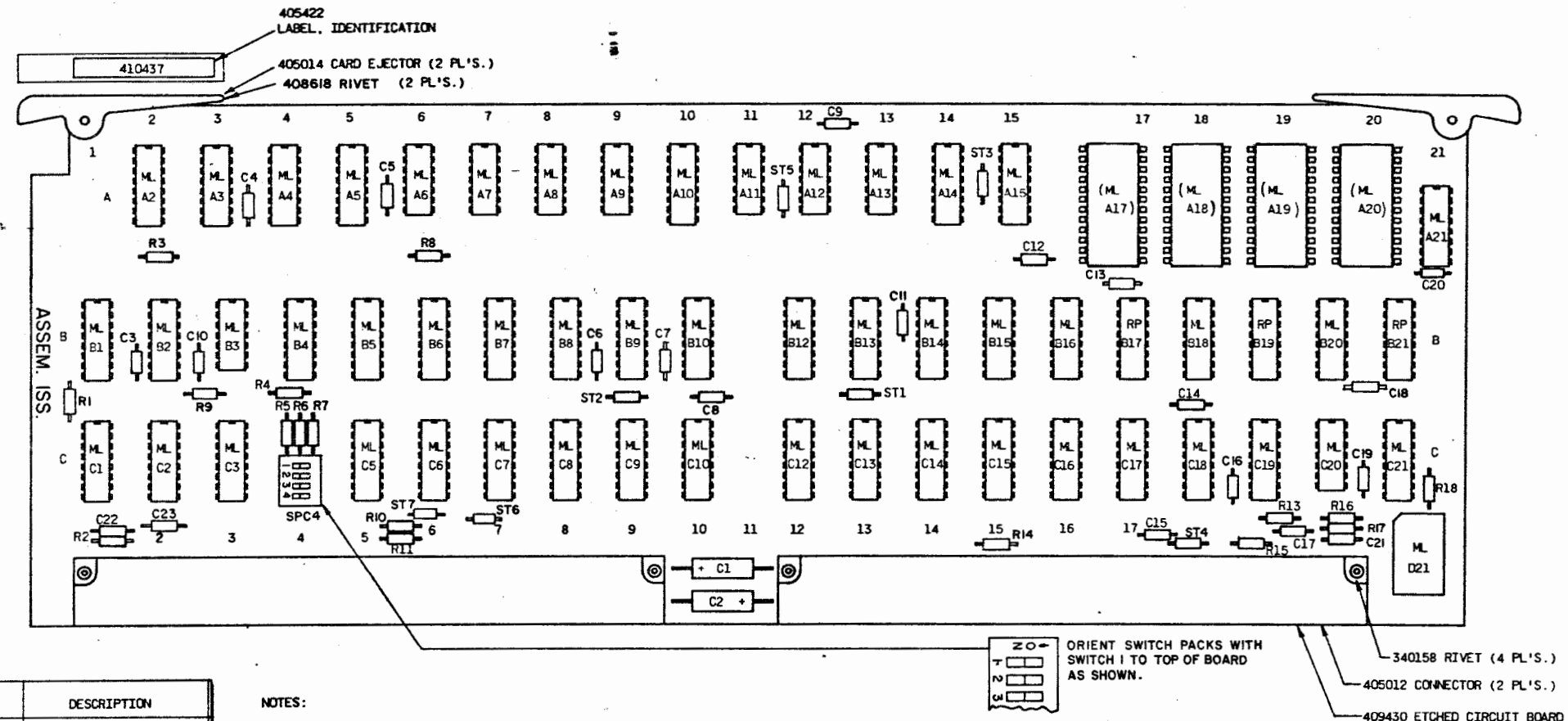
REVISIONS						
CUSTOMER IDENTIFICATION	ISSUE	VERSION	ASSOCIATED NOTE	DRAWING ISSUE	CONFORMANCE DATE	AUTH. NO.
1	B	1	1	3-2-75	24591R	
1	B	2	2		16817	
1	B	3	3		11991	
1	B	4	4		18017	
1	B	5	5	3-21-77	18325	
1	B	6	6		18595	

CIRCUIT CARD		
CC 411		
CIU / PIT / SID ASSEMBLY		
APPROVALS		
PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.
ENGR. JAB	DSGMR.	
DRAWN		DATE 3-19-76
E - NUMBER		
SD - CD NO 4411		
R & D FILE NO. 6-167.172AA		
TELETYPE		
410411		

REF. DESIG.	PART NO. REQ.	QTY	DESCRIPTION
C1	310931		CAPACITOR, 47MFD., 20V
C2			SAME AS C1
C3	405324		CAPACITOR, 0.1 MFD, 50V
C4			SAME AS C3
C5			SAME AS C3
C6			SAME AS C3
C7			SAME AS C3
C8			SAME AS C3
C9			SAME AS C3
C10			SAME AS C3
C11			SAME AS C3
C12			SAME AS C3
C13			SAME AS C3
C14			SAME AS C3
C15			SAME AS C3
C16			SAME AS C3
C17			SAME AS C3
C18			SAME AS C3
C19			SAME AS C3
C20			SAME AS C3
C21			SAME AS C3
C22			SAME AS C3
C23			SAME AS C3
R1	320276		RESISTOR, 4700, 1/4W, 5%
R2			SAME AS R1
R3	315957		RESISTOR, 3.3K, 1/4W, 5%
R4			SAME AS R1
R5			SAME AS R3
R6			SAME AS R3
R7			SAME AS R3
R8			SAME AS R1
R9			SAME AS R3
R10			SAME AS R1
R11			SAME AS R1
R13	320784		RESISTOR, 2700, 1/4W, 5%
R14			SAME AS R3
R15			SAME AS R3
R16	315952		RESISTOR, 8200, 1/4W, 5%
R17	318802		RESISTOR, 2200, 1/4W, 5%
R18	333405		RESISTOR, 1200, 1/4W, 5%

REF. DESIG.	PART NO.	DESCRIPTION
MLA2	339174	IC, HEX LATCH
MLA3	339163	IC, 4-BIT BINARY CTR
MLA4	405060	IC, 256 X 4 BIT ROM
MLA5		SAME AS MLA3
MLA6	339437	IC, QUAD NAND BUFF
MLA7		SAME AS MLA6
MLA8	339003	IC, TRI-3 IN NAND
MLA9	339404	IC, HEX INVERTER
MLA10	339476	IC, DUAL FLIP-FLOP
MLA11		SAME AS MLA8
MLA12	339408	IC, QUAD 2 IN AND
MLA13	339438	IC, QUAD NAND BUFF
MLA14	405058	IC, 32 X 8 BIT ROM
MLA15		SAME AS MLA3
MLA21	339707	IC, ECL TRI OR/NOR
MLB1	339145	IC, 1 OF 10 DECODER
MLB2		SAME AS MLA3
MLB3	339432	IC, QUAD 2 IN OR
MLB4	339347	IC, 6-BIT COMPARE
MLB5		SAME AS MLA2
MLB6		SAME AS MLA2
MLB7		SAME AS MLA2
MLB8		SAME AS MLA2
MLB9		SAME AS MLA4
MLB10		SAME AS MLA3
MLB12	339608	IC, QUAD 80 BIT SR
MLB13		SAME AS MLB12
MLB14		SAME AS MLA2
MLB15	339175	IC, QUAD LATCH
MLB16	339475	IC, QUAD LATCH
MLB18	339166	IC, 8-BIT SR
MLB20	339776	IC, ECL HEX D LATCH
MLC1	339151	IC, 8-1 MUX
MLC2	405059	IC, 32 X 8 BIT ROM
MLC3	339837	IC, HX BUS RCVR
MLC5	339838	IC, QUAD BUS XCVR
MLC6		SAME AS MLB12
MLC7	339157	IC, QUAD 2-1 MUX

NOTE: MANUFACTURE PER MR2028 (CLASS AAA/K/T/2)



NOTES:

- THIS CARD MUST BE ASSEMBLED USING 409430 BOARD, ISSUE 3A OR LATER.
- ON COMPONENT SIDE, CUT CONDUCTOR BETWEEN MLA14-15 AND MLA15-2.
- ON CKT. SIDE, CUT CONDUCTOR AT MLC20-8.
- ON COMPONENT SIDE, ADD A STRAP FROM MLA14-15 TO MLA14-8.
- ON COMPONENT SIDE, ADD A STRAP FROM MLC15-14 TO SIDE OF ST-3 THAT PREVIOUSLY WAS CONNECTED TO MLC20-8.

(REF. C.O.A. 16509)

- DELETE R12 FROM DWG. AND PARTS LIST.
- FOR CONV. FROM CUST. ISSUE 1A TO 1B CIRCUIT CHANGES FROM NOTE 1 PUT INTO PRINTED CIRCUIT BOARD PATTERN (BOARD ISSUE 4A).
- FOR CONVERSION FROM CUST. ISSUE 1A TO 2A ADD THE FOLLOWING STRAPS: FROM MLB10-1 TO RPB17-3, FROM MLC13-14 TO RPB17-7, FROM MLA3-9 TO +5V (MLA3-16), FROM MLA5-9 TO +5V (MLA5-16), FROM MLA15-1 TO +5V (MLA15-16).

NOTE 5: FOR CONVERSION OF CUST. TO ISSUE 2A TO 2B PULL-UP RESISTOR RPB17-3 CONNECTED TO PINS MLA2-1, MLA10-3, MLA10-7, MLB5-1, MLB6-1, MLB7-1, MLB8-1, MLA10-1, MLB14-1, MLB15-1, MLC15-1, MLC18-1, AND +5V CONNECTED TO PINS MLA3-9, MLA5-9, MLA15-1, PUT INTO PRINTED CIRCUIT BOARD PATTERN (BOARD ISSUE 5A). PULL-UP RESISTOR RPB17-7 CONNECTED TO MLC13-14 BY A WIRE ON THE COMPONENT SIDE. MLA14-15 CONNECTED TO GND, MLA14-8, BY A WIRE ACROSS OPEN LAND ON CIRCUIT SIDE.

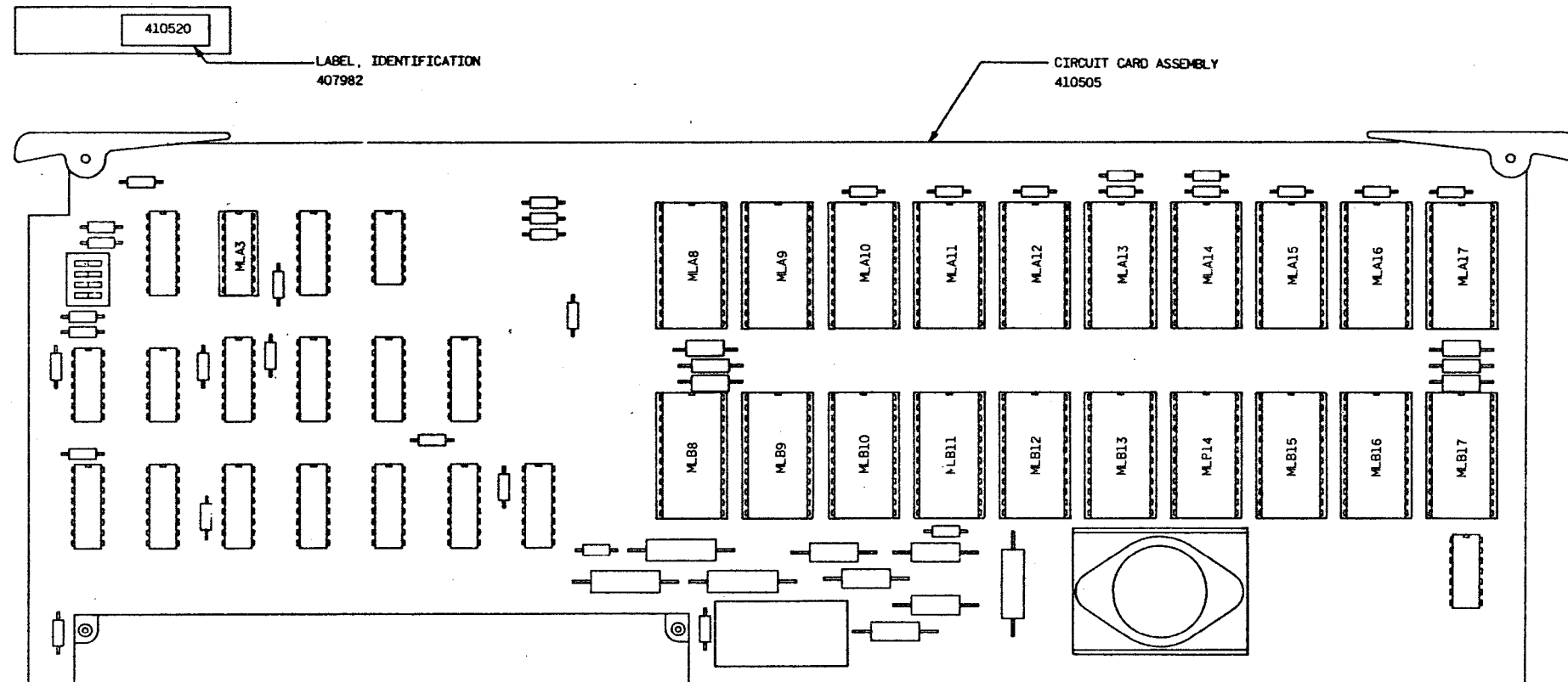
REVISIONS					
CUSTOMER IDENTIFICATION	ISSUE	VERSION	ASSOCIATED NOTE	DRAWING ISSUE	CONFORMANCE DATE
1	A	1		1	8-18-76
1	A	2		2	16659
1	A	3		3	11991
1	B	3		4	7-13-77
2	A	4		5	1-2-78
2	B	5		6	2-15-78
2	B	7		7	20170RC
2	B	8		8	18595

CIRCUIT CARD		
CC 437		
DIO ASSEMBLY FOR 40C400 CONTROLLER		
APPROVALS		
PROJ. SUFV.	PROJ. DIR.	MFG. REL. COMPL.
ENGR. J.M.G.	DSGMR.	
DRAWN	DATE	
E - NUMBER		
SD - CD NO 4430		
R & D FILE NO 2-176 172AA		
TELETYPE		
410437		

[illegible]

NOTE: MANUFACTURE PER MR2001

SCREEN PER MR2028 AAA/II/T/2



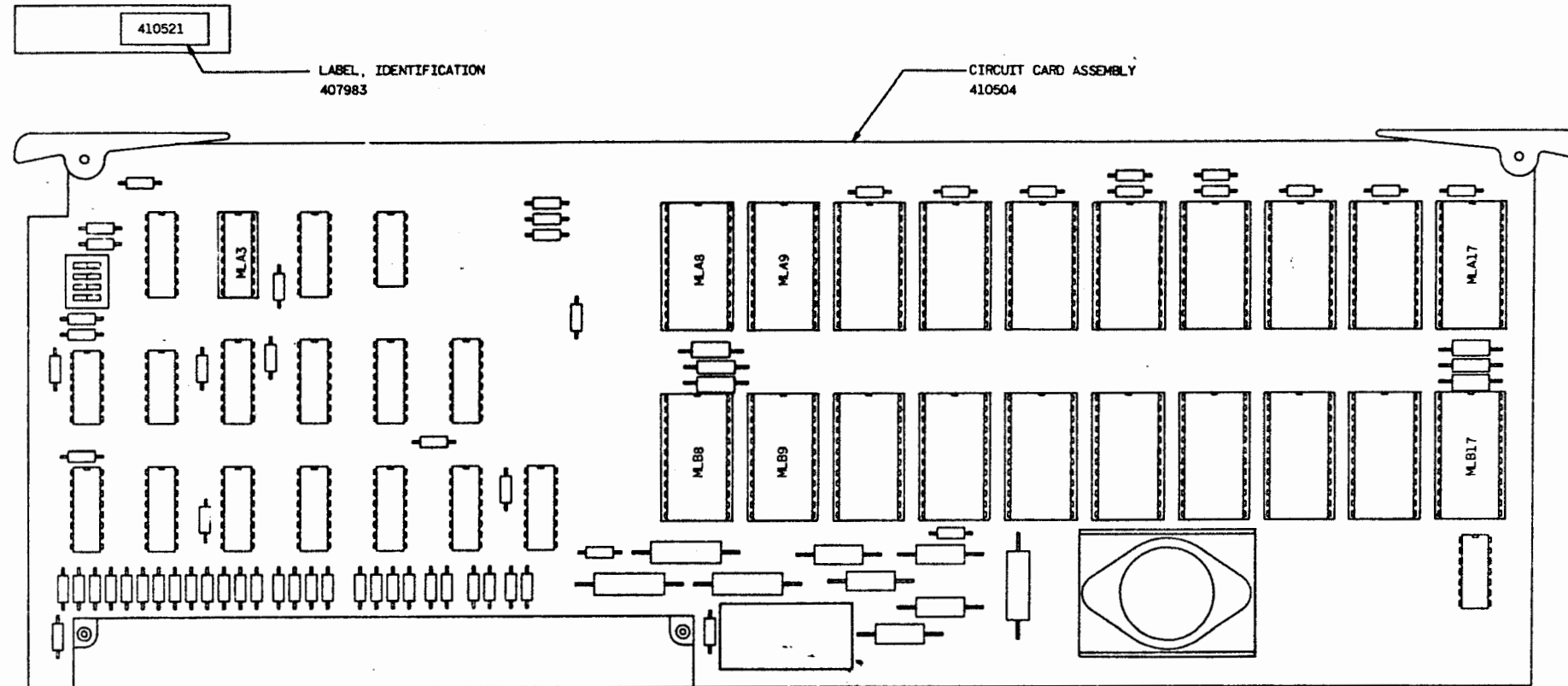
1. FOR CONVERSION TO CUSTOMER I.D. 2A,
451180, 451181 & 451184 - 451187 EPROMS
CHANGED FROM ISSUE 1 TO ISSUE 2.
2. FOR CONVERSION TO CUSTOMER I.D. 3A,
451176, 451190, & 451191 EPROMS CHANGED
FROM ISSUE 1 TO ISSUE 2.
3. FOR CONVERSION TO CUSTOMER I.D. 4A,
451186 CHANGED TO ISSUE 3.
4. FOR CUSTOMER ID ISSUE 5A REFER TO NOTE 1
ON 410505 CARD ASSEMBLY.

SIMILAR TO:

CUSTOMER'S IDENTIFICATION			REVISIONS			
ISSUE	INF.	VERSION	ASSOCIATED NOTE	ISSUE	CONFORMANCE DATE	AUTH. NO.
1	A	—		1	3-21-78	25469R
2	A	1		2	5-19-78	20591
3	A	2		3	6-6-78	20663
4	A	3		4	6-28-78	20740
5	A	4		5	3-2-79	22330
P						
CIRCUIT CARD						
MC						
10K ROM ASSEMBLY						
APPROVALS						
PROJ. SUPV.		PROJ. DIR.		MFG. REL.		
ENGR. RVP		DSGMR.		DATE		
E - NUMBER						
SD - CD NO. 6500						
R & D FILE NO. G-65.172AA						
TELETYPE						
						
410520						

REF. DESIG.	PART NO. REQ.	QTY	DESCRIPTION
	410524	1	CIRCUIT CARD ASSEMBLY
	407983	1	LABEL IDENTIFICATION
MLA3	451002	1	256 x 4 ROM ISS. 1
MLA8	451002	1	1024 x 8 ROM ISS. 1
MLB8	451003	1	1024 x 8 ROM ISS. 1
MLA9	451500	1	1024 x 8 ROM ISS. 1
MLB9	451501	1	1024 x 8 ROM ISS. 1
MLA17	451192	1	1024 x 8 ROM ISS. 2
MLB17	451193	1	1024 x 8 ROM ISS. 2

NOTE: MANUFACTURE PER MR2001
SCREEN PER MR2028 AAA/II/T/2



- NOTE 1. SELF TEST ROMS 451000-1 WERE
"CHANGED" TO 451500-1
2. FOR CONVERSION TO CUSTOMER
I.D. ISSUE 3A, 451192 & 451193
EPROMS CHANGED TO ISSUE 2.
3. FOR CUSTOMER ID ISSUE 4A REFER TO NOTE 1
ON 410504 CARD ASSEMBLY.

SIMILAR TO:

REVISIONS					
CUSTOMER LOCATION DATE	ISSUE VERSION	ASSOCIATED NOTE	DATE ISSUE	CONFORMANCE DATE	AUTH. NO.
1	A		3-21-78	25469 R	
2	A	1	6-15-78	20474	
3	A	2	8-23-78	20839	
4	A	3	3-2-79	22330	

CIRCUIT CARD	
MC	2K +1K ROM W/BUS R ASSEMBLY
APPROVALS	
PROJ. SUPV.	PROJ. DR. MFG. REL. COMPL.
ENGR. RVP	DSGNR.
DRAWN	DATE
E - NUMBER	
SD - CD NO. 4500	
R & D FILE NO. G-65.172AA	
TELETYPE	
410521	

ORIGINAL USE
FINAL
DIRECT

THIS MATERIAL IS TO BE TREATED AS TELETYPE CORPORATION PROPRIETARY INFORMATION AND IS NOT TO BE DELIVERED TO ANY ONE OUTSIDE OF TELETYPE CORPORATION, EXCEPT UNDER STRICTEST CONFIDENCE AND THEN ONLY WITH A FORMAL CONTRACT, PURCHASE ORDER, OR REQUEST TO QUOTE. ANYONE OUTSIDE OF TELETYPE CORPORATION WHO ACCEPTS THIS MATERIAL AGREES THAT: THIS MATERIAL IS NOT TO BE REPRODUCED IN ANY FORM WITHOUT THE WRITTEN APPROVAL OF TELETYPE CORPORATION, AND PARTS AND/OR APPARATUS IN ACCORDANCE WITH OR SIMILAR TO THIS MATERIAL ARE NOT TO BE MANUFACTURED FOR OTHERS EXCEPT ON THE WRITTEN APPROVAL OF THE TELETYPE CORPORATION.

[illegible]

1	4-5-78	25258 R
ISSUE	DATE	AUTH. NO.

REVISIONS

APPROVALS		
PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.
		

ENGR	RVP	DSGNR
DRN		DATE

E-NUMBER

PROD. NO. 408968 (1 OF 4)

R&D FILE G-65.172AA

TELETYPE



408968 (1)

197

TELETYPE CORPORATION - COMPANY PRIVATE

SCALE /

FINISH	HEAT TREAT	MATERIAL SPECIFICATION

[illegible]

CARD POSITION		CARD NO.		410411
5		5		

A21	B1	B2	B3	B4	B5	B6	B7	B8
● 1 ZZ	A V	F G	● L	AA ●	P	●	S	T
2 ZZ	W	H	M	●	Q	●	S	T
3 ZZ	X	Y	M	●	Q	●	S	T
4 ZZ	B	I	●	●	R	●	S	T
5 ZZ	C	J	●	●	R	●	S	T
6 ZZ	D	Z	●	●	R	●	S	T
7 ZZ	E	K	N	U		●		
8 ZZ								●
9 ZZ								

CON OVER

SIMILAR TO:

"OTHER" SWITCH PAKS

CARD POSITION	6	CARD NO.
		410411

A21	B1	B2	B3	B4	B5	B6	B7	B8
● ZZ ZZ ZZ ZZ ZZ ZZ ZZ ●	A V W X B C D E	F G H Y I J Z K	● L M M ● ● ● N	AA ● ● ● ● ● U	P P Q Q R R ● ●	● ● ● ● ● ● ● ●	S S S S S S ●	T T T T T T T ●

NO. 2

TELETYPE CORPORATION - COMPANY PRIVATE

SCALE /

CARD POSITION	I/O SOCKET	CABLE NO.	DEVICE	TERMINAL I.D.
3	J301	402236	MONITOR	
4	J307	407526	CASSETTE (CD-1)	
4	J308	407526	CASSETTE (CD-2)	
4	J310	407585	PRINTER	
4	J309	407582	KEYBOARD	
5	J311	407526	CASSETTE (CD-3)	
6	J305	USER	LINE INTERFACE	

NOTE:

1. THE OFF AND ON POSITION OF SOME SWITCH PACKS MAY BE REVERSED.
LOOK FOR THE ON MARKING ON EACH SWITCH WHEN SETTING OPTIONS.

ORIGINAL USE	FINAL DIRECT
1. CARD	

40C435AEE09I WITH
ADDITIONAL 410406 CARD

THIS MATERIAL IS TO BE TREATED AS TELETYPE CORPORATION PROPRIETARY INFORMATION AND IS NOT TO BE DELIVERED TO ANY ONE OUTSIDE OF TELETYPE CORPORATION, EXCEPT UNDER STRICTEST CONFIDENCE AND THEN ONLY WITH A FORMAL CONTRACT, PURCHASE ORDER, OR REQUEST TO QUOTE. ANYONE OUTSIDE OF TELETYPE CORPORATION WHO ACCEPTS THIS MATERIAL AGREES THAT: THIS MATERIAL IS NOT TO BE REPRODUCED IN ANY FORM WITHOUT THE WRITTEN APPROVAL OF TELETYPE CORPORATION, AND PARTS AND/OR APPARATUS IN ACCORDANCE WITH OR SIMILAR TO THIS MATERIAL ARE NOT TO BE MANUFACTURED FOR OTHERS EXCEPT ON THE WRITTEN APPROVAL OF THE TELETYPE CORPORATION.

1		
ISSUE	DATE	AUTH. NO.
REVISIONS		
APPROVALS		
PROJ. SUPV. <i>[Signature]</i>	PROJ. DIR. <i>[Signature]</i>	MFG. REL. COMPL. <i>[Signature]</i>
ENGR	RVP	DSGNR
DRN	DATE	
E-NUMBER		
PROD. NO. 408968 (2 OF 4)		
R&D FILE 6-65.172AA		
		
408968 (2)		

NOTES:

1). DEFINITION OF OPTIONS

A. ECHO COPY BY PRINTER

410411 - B1-1

PRINTER TO COPY DATA AS IT IS SENT FROM THE TERMINAL - ON

PRINTER TO COPY DATA ECHOED BACK ON THE RECEIVE LINE - OFF

B. SEND ETX ON PREMATURE END OF MESSAGE

B1-5

ETX SENT - ON

NO ETX SENT - OFF

C. COLON IS LOWER CASE ON THE KEYBOARD AND SEMI-COLON UPPER CASE

B1-6

ENABLE - ON

REVERSED - OFF

D. KEYBOARD ON LINE TRANSMITS BLIND

B1-7

KEYBOARD TRANSMITS BLIND - ON

DISPLAY COPIES KEYBOARD DATA - OFF

E. DISPLAY RECEIVED ESCAPE SEQUENCES

B1-8

ESCAPE SEQUENCES DISPLAYED - ON

ESCAPE SEQUENCES PERFORMED - OFF

F. PRINTER REQUIRED TO TRANSMIT ON-LINE

B2-1

PRINTER REQUIRED - ON

PRINTER NOT REQUIRED - OFF

G. SEND ON-LINE EXTENDED KEYBOARD CHARACTERS (KBD ON-LINE MODE)

B2-2

SEND EXTENDED CHARACTERS AS ESCAPE SEQUENCES - ON

IGNORE EXTENDED KEYBOARD CHARACTERS - OFF

H. MONITOR TAPE REQUIRED TO TRANSMIT ON-LINE

B2-3

MONITOR TAPE REQUIRED - ON

MONITOR TAPE NOT REQUIRED - OFF

I. AUTOMATIC PAGING ON PRINTER (54 LINES - PAGE)

B2-5

PAGING "F"'S SENT TO PRINTER - ON

NO PAGING - OFF

J. PRINTER OPTIONED FOR DOUBLE LINE FEED (USED WITH OPTION 1)

B2-6

PRINTER OPTIONED FOR DOUBLE LINE FEED - ON

PRINTER OPTIONED FOR SINGLE LINE FEED - OFF

K. KEEP RECEIVED LETTERS (SHIFT - IN) AND FIGURES (SHIFT - OUT) CHARACTERS (5 LEVEL OPERATION ONLY)

B2-8

DO NOT DISCARD S_0 , S_1 CHARACTERS - ON

DISCARD S_0 , S_1 CHARACTERS - OFF

L. PRINTER SELECT ALSO SELECTS RECEIVE TAPE

B3-2

RECEIVE TAPE SELECTED WITH PRINTER - ON

PRINTER ONLY SELECTED - OFF

M. TERMINAL PARITY

B3-3

B3-4	ON	OFF
ON	ODD PARITY	EVEN PARITY
OFF	ODD PARITY	NO PARITY

N. DISPLAY STAYS IN RECEIVE AT END OF MESSAGE,

B3-8

DISPLAY STAYS IN RECEIVE - OFF

DISPLAY GOES TO LOCAL - ON

P. SEND TAPE LOCATION

B5-1

B5-2	ON	OFF
ON	J311	J308
OFF	J307	NO SEND TAPE

Q. RECEIVE TAPE LOCATION

B5-3

B5-4	ON	OFF
ON	J311	J308
OFF	J307	NO REC. TAPE

R. MONITOR TAPE LOCATION

B5-5

B5-6	ON	OFF
ON	J311	J308
OFF	J307	NO MON. TAPE

REVISIONS

ISSUE	DATE	AUTH. NO.
1		

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.
ENGR.	DSGNR.	
DRN.	DATE	
R & D FILE G-65,172AA		
S-NUMBER 408968 (3 OF 4)		

TELETYPE



408968 (3 OF 4)

NOTES (CONTINUED)

1). DEFINITION OF OPTIONS

S & T STATION IDENTIFY (POLL-SELECT)

MARKING BIT - SWITCH ON

SPACING BIT - SWITCH OFF

	BIT	1	2	3	4	5	6	7
1st CHARACTER	B7-1	B7-2	B7-3	B7-4	B7-5	B7-6	B7-7	
2nd CHARACTER	B8-1	B8-2	B8-3	B8-4	B8-5	B8-6	B8-7	

NOTE: BOTH SWITCHES B7-8 AND B8-8 MUST BE OFF

U. DISPLAY GOES RECEIVE ON-LINE AFTER SEND ON-LINE

B4-8

ON-RECEIVE ON SEND

OFF-DISPLAY GOES OFF AFTER SEND

V. ISOCHRONOUS OPERATION

B1-2

TERMINAL OPERATES ISOCHRONOUSLY ON LINE - ON

TERMINAL OPERATES ASYNCHRONOUSLY ON-LINE - OFF

W. DATA TERMINAL READY CONTROL

B1-3

DTR OFF WHEN RECEIVE BUFFER CONTAINS 204

CHARS. AND BACK ON WHEN THE BUFFER
CONTAINS ONLY 25 CHARS. - ON

DTR NOT CONTROLLED BY REC. BUFFER - OFF

X. LINE WRAP

B1-4

DISPLAY WRAPS WHEN CURSOR REACHES

END OF LINE - ON

DISPLAY DOES NOT WRAP - OFF

Y. REJECT NULLS

B2-4

TERMINAL REJECTS INCOMING NULLS - ON

TERMINAL DOES NOT REJECT NULLS - OFF

Z. HOME ON SEND

B2-7

CURSOR GOES HOME BEFORE SENDING FROM THE DISPLAY - ON

DISPLAY SENDS FROM CURSOR - OFF

AA. STOP BITS IN 5-LEVEL OPERATION

B4-1

TERMINAL SENDS/RECEIVES 1.5 STOP BITS ON

TERMINAL SENDS/RECEIVES 1 STOP BIT OFF

ZZ. TRANSMISSION/RECEPTION SPEEDS

5-LEVEL OPERATION

A21-6	A21-7	A21-8	BAUD RATE
OFF	OFF	OFF	50
ON	OFF	OFF	75
OFF	ON	OFF	100
ON	ON	OFF	110
OFF	OFF	ON	150
ON	OFF	ON	300
OFF	ON	ON	450
ON	ON	ON	600

8-LEVEL OPERATION

A21-2	A21-3	A21-4	A21-5	BAUD RATE
OFF	OFF	OFF	ON	50
OFF	OFF	ON	ON	75
OFF	ON	OFF	ON	100
OFF	ON	ON	ON	100
ON	OFF	OFF	ON	150
ON	OFF	ON	ON	300
ON	ON	OFF	ON	450
ON	ON	ON	ON	600
OFF	ON	ON	OFF	900
ON	OFF	OFF	OFF	1200
ON	OFF	ON	OFF	1800
ON	ON	OFF	OFF	2400

REVISIONS

ISSUE	DATE	AUTH. NO.
1		

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.

ENGR.	DSGNR.
DRN.	DATE

R & D FILE G-65.172AA

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